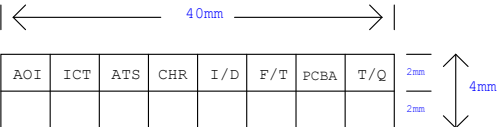


Project : MT50IN Schematics Rev : 01

Intel Ivy Bridge CPU + Intel Panther Point Chipset + nVidia N13P-GL

Page	Content
01	Cover Page
02	System Block Diagram
03	Power Diagram
04	Power Sequence
05	GPIO & Power Consumption
06	Ivy Bridge_DMI, FDI, PEG
07	Ivy Bridge_DDR3
08	Ivy Bridge_Power
09	Ivy Bridge_GND
10	Ivy Bridge_Reserved
11	DDR3 SO-DIMM Channel A,B
12	Panther Point_RTC,HDA,SATA
13	Panther Point_PCIE,CLK,SMBus
14	Panther Point_LVDS,CRT,Manage
15	Panther Point_PCI,USB
16	Panther Point_GPIO,MISC
17	Panther Point_Power1
18	Panther Point_Power2
19	Panther Point_GND
20	LVDS/Webcam
21	CRT/HDMI
22	MiniCard/LED/BT/HDD/ODD/MSATA
23	USB 3.0 /G-Sensor/TPM
24	Audio Codec (ALC269)
25	Card Reader (RTS5159-GR)
26	LAN(RTL8111E/8105E)
27	EC (IT8518)/BIOS/KBC
28	Power Switch/Hole/FAN
29	DC/Charger OZ8682
30	+VCC/+GFX_Core(ISL95836HRTZ)
31	+1.5VS (OZ80112)/+0.75VS_DDR
32	+5VA/+1.05V (OZ8153)
33	+3.3VA/+0.85V/+1.8V
34	VGA_Core (OZ8292)
35	VGA_PCIE
36	VGA HDMI/LVDS/DVI
37	VGA MEM_Interface
38	VGA Power 1
39	VGA Power 2
40	VGA Thermal/CRT/XTAL
41	VGA DDR3_MEM_A
42	VGA DDR3_MEM_B
43	Connector List/SKU Select
44	Change Notes

Phase	Revision History	
A	02/18/2012	Initial REV.A
B	03/29/2012	REV.B
01	05/21/2012	Risk buy REV 01



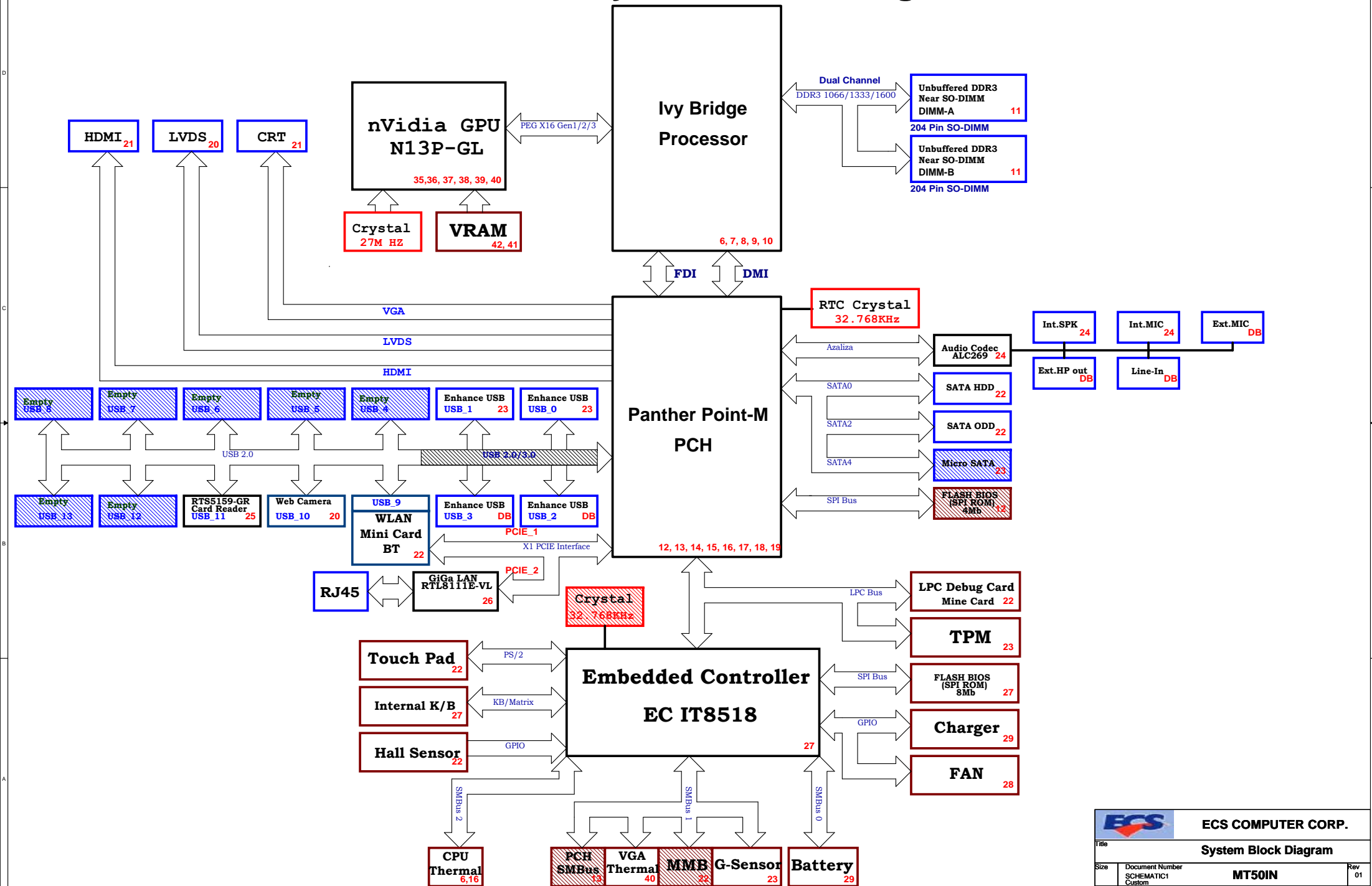
PCB
PCB
15BFR7- 011000

MT50IN MB Ver:01
P/N:15BFR7- 011000
PCB M/B MT50IN1.V.01 255.58*194.07*1.2mm.6L LEAD-FREE.GREEN

MT50IN1 Rev. P/N List :

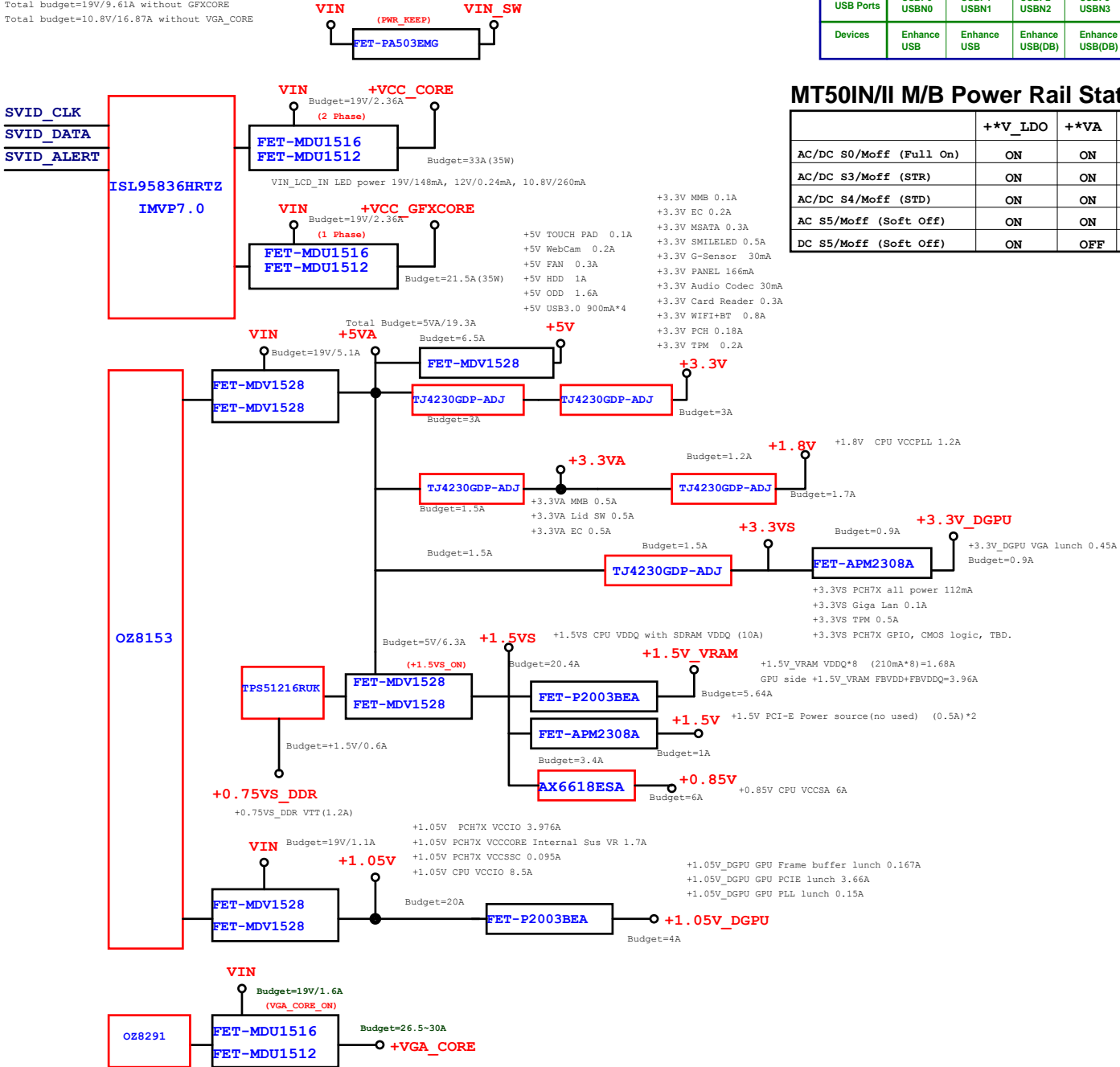
Phase Revision	M/B PCB P/N	USB PCB P/N	SW PCB P/N	LED PCB P/N	
Initial REV.A					
REV.B	15BFR7-010200	15BFR7-050210	15BFR7-050212	15BFR7-050211	
REV.01	15BFR7- 011000	15BFR7-051001	15BFR7-051000	15BFR7-051002	
REV.A1		15BFR6-050100	15BFR6-050101		

Chief River System Block Diagram



Power Block Diagram

CPU (35W)
Total budget=19V/9.61A without GFXCORE
Total budget=10.8V/16.87A without VGA_CORE



USB Port Devices Table

USB Ports	USB0 USBN0	USB1 USBN1	USB2 USBN2	USB3 USBN3	USB4 USBN4	USB5 USBN5	USB6 USBN6	USB7 USBN7	USB8 USBN8	USB9 USBN9	USB10 USBN10	USB11 USBN11	USB12 USBN12	USB13 USBN13
Devices	Enhance USB	Enhance USB	Enhance USB(DB)	Enhance USB(DB)	None	None	Disable	Disable	Disable	WLAN BT	Web Camera	Card Reader	None	None

MT50IN/II M/B Power Rail State :

	++V_LDO	++VA	++VS	++V	CLK
AC/DC S0/Moff (Full On)	ON	ON	ON	ON	ON
AC/DC S3/Moff (STR)	ON	ON	ON	OFF	Only MCH BCLK
AC/DC S4/Moff (STD)	ON	ON	OFF	OFF	OFF
AC S5/Moff (Soft Off)	ON	ON	OFF	OFF	OFF
DC S5/Moff (Soft Off)	ON	OFF	OFF	OFF	OFF

System Power Rail

Voltage Name	Control Pin	S0	S1	S3	S4	S5
+VXG_CORE	GFX_IMON	ON	ON	ON	OFF	OFF
+VCC_CORE	+VCC_CORE_ON	ON	ON	ON	OFF	OFF
+V1.05S	+V1.5S_ON	ON	ON	ON	OFF	OFF
+V1.5S	+V1.5S_ON	ON	ON	ON	OFF	OFF
+V3.3S	+V3.3S_ON	ON	ON	ON	OFF	OFF
+V5S	+V5S_ON	ON	ON	ON	OFF	OFF
+V1.1S_VTT	+V5S	ON	ON	ON	OFF	OFF
+V1.8S	+V5S	ON	ON	ON	OFF	OFF
+V1.1S	+V5S	ON	ON	ON	OFF	OFF
+V0.75DDR	+V1.5	ON	ON	OFF	OFF	OFF
+V1.5	+V1.5_ON	ON	ON	OFF	OFF	OFF
+V3.3	+V3.3_ON	ON	ON	OFF	OFF	OFF
+V5	+V5_ON	ON	ON	OFF	OFF	OFF
VIN_SW	PWR_KEEP	ON	ON	OFF	OFF	OFF
+V3.3_AUX	AC:follow VIN up	ON	ON	ON	ON	ON
+V5_AUX	DC:AUX_ON	ON	ON	ON	OFF	OFF
	AC:follow VIN up	ON	ON	ON	ON	ON
	DC:AUX_ON	ON	ON	ON	OFF	OFF

CPU Huron River
Power Rail

		Laptop Mode				
		S0	S1	S3	S4	S5
VCC	+VCC_CORE	ON	ON	OFF	OFF	OFF
VTT	+V1.1S	ON	ON	OFF	OFF	OFF
VXG	+VCC_CORE	ON	ON	OFF	OFF	OFF
VCCPLL1	+V1.8S	ON	ON	OFF	OFF	OFF
VDDQ	+V1.5S	ON	ON	OFF	OFF	OFF

SB Ixex Peak
Power Rail

		Laptop Mode				
		S0	S1	S3	S4	S5
VCCACLK	+V1.1S	ON	ON	ON	OFF	OFF
VCCCORE	+V1.1S	ON	ON	ON	OFF	OFF
VCCAPLLEXP	+V1.1S	ON	ON	ON	OFF	OFF
VCCIO	+V1.1S	ON	ON	ON	OFF	OFF
VCC3_3	+V3.3S	ON	ON	ON	OFF	OFF
VCCFDPLL	+V1.1S	ON	ON	ON	OFF	OFF
VCCVRM	+V1.8S	ON	ON	ON	OFF	OFF
VCCPNAND	+V1.8S	ON	ON	ON	OFF	OFF
VCCDMI	+V1.1S_VTT	ON	ON	ON	OFF	OFF
VCCALVDS	+V3.3S	ON	ON	ON	OFF	OFF
VCCCTX_LVDS	+V1.8S	ON	ON	ON	OFF	OFF
VCCADAC	+V3.3S	ON	ON	ON	OFF	OFF
V5REF	+V5S	ON	ON	ON	OFF	OFF
VCCADPLL	+V1.1S	ON	ON	ON	OFF	OFF
VCCSATAPLL	+V1.1S	ON	ON	ON	OFF	OFF
V_CPU_IO	+V1.1S	ON	ON	ON	OFF	OFF
VCCADPLLA	+V1.1S	ON	ON	ON	OFF	OFF
VCLAN	+V1.1S	ON	ON	ON	OFF	OFF
VCCSUSDA	+V3.3A	ON	ON	ON	ON	ON
VCCSUS3_3	+V3.3A	ON	ON	ON	ON	ON
VCCRTC	+V3A	ON	ON	ON	ON	ON
V5REF_SUS	+V5A	ON	ON	ON	ON	ON



ECS COMPUTER CORP.

Power Diagram			
File	Document Number	MT50IN	Rev 01
Size	Custom		
Date:	Friday, June 15, 2012	Sheet	3 of 44

System Power On Sequence (TBD)

PCH GPIO	
GPIO0	S_GPIO
GPIO1	SMC_RUNTIME_SCI#
GPIO2	MPC_PWR_CTRL#
GPIO3	SATA_ODD_DA#
GPIO4	EXTTS_SNI_DRV0_PCH
GPIO5	EXTTS_SNI_DRV1_PCH
GPIO6	PCH_TACH2
GPIO7	PCH_TACH3
GPIO8	COLOR_ENGINE_EN
GPIO9	USB_OC#_10_11
GPIO10	USB_OC#_12_13
GPIO11	PCH_GPIO11
GPIO12	PCH_GPIO12
GPIO13	NC
GPIO14	USB_OC#_13_14
GPIO15	HOST_ALERT#1
GPIO16	SATA_DET#4
GPIO17	PCH_TACH0
GPIO18	CLK_PCIE_LAN_REQ#_R
GPIO19	BBS_BIT0
GPIO20	NC
GPIO21	SATA_DET0#
GPIO22	BIOS_REC
GPIO23	NC
GPIO24	HOST_ALERT#2
GPIO25	NC
GPIO26	NC
GPIO27	PCH_GPIO27
GPIO28	PLL_ODVR_EN
GPIO29	PM_SLP_LAN#
GPIO30	SUS_PWR_ACK_R
GPIO31	AC_PRESENT
GPIO32	PM_CLKRUN#
GPIO33	@1K to GND
GPIO34	GPIO34
GPIO35	PLTRST#_PCH
GPIO36	PCH_GPIO36
GPIO37	FDI_OVRVLTG
GPIO38	MFG_MODE
GPIO39	GFX_CRB_DET
GPIO40	USB_OC#_2_3
GPIO41	USB_OC#_4_5
GPIO42	USB_OC#_6_7
GPIO43	USB_OC#_8_9
GPIO44	NC
GPIO45	NC
GPIO46	NC
GPIO47	-CLKREQ_GFX
GPIO48	TEST_SET_UP
GPIO49	PCH_GPIO49
GPIO50	DGPU_HOLD_RST
GPIO51	BBS_BIT1
GPIO52	PCI_REQ#2
GPIO53	NC
GPIO54	PCI_REQ#3
GPIO55	STP_A160VR
GPIO56	NC
GPIO57	TEST_DET
GPIO58	SMB1_CLK_EC
GPIO59	USB_OC#_0_1
GPIO60	RST_GATE
GPIO61	PM_SUS_STAT#
GPIO62	NC
GPIO63	NC
GPIO64	CLK_27M_TP
GPIO65	USB_48M_TP
GPIO66	LAN25M_TP
GPIO67	SEL24_48M_P
GPIO68	SATA_ODD_PWRGT
GPIO69	@1.5K to GND
GPIO70	100K to +3.3V
GPIO71	100K to +3.3V
GPIO72	PM_BATLOW#
GPIO73	CLK_MINI1_OE#_R
GPIO74	PCH_GPIO74
GPIO75	SMB1_DAT_EC

ITE8518 GPIO Pin Definition List	
GPA0	BTL_BEEP
GPA1	EC_BL_PWM
GPA2	WLAN_ON
GPA3	WEBCAM_EN
GPA4	RF_LED
GPA5	+0.85V_ON
GPA6	OPTION4
GPA7	BT_EN#
GPB0	SENBAT_V
GPB1	INT1
GPB2	PWR_LEVEL
GPB3	SMBCLK_EC0
GPB4	SMBDAT_EC0
GPB5	H_A20GATE
GPB6	H_RCIN#
GPB7	OPTION2
GPC0	+1.8V_ON
GPC1	SMBCLK_EC1
GPC2	SMBDAT_EC1
GPC3	SAFETY
GPC4	+3.3V_ON
GPC5	+5V_ON
GPC6	+1.05V_ON
GPC7	PM_PWRBTN#
GPD0	AC_IN
GPD1	OPTION1
GPD2	BUF_PLT_RST#
GPD3	EC_SCI#
GPD4	SATA_ODD_PWRGT_EC +3.3V_DGPU_ON
GPD5	AC_PRESENT
GPD6	+1.5VS_ON
GPD7	Battery_MA#
GPE0	PM_RSMRST#
GPE1	FNOPTION
GPE2	PM_AFWROK
GPE3	OPTION5
GPE4	PWRON_EC
GPE5	OPTION3
GPE6	SATA_LED1#
GPE7	MUTE_AMP#
GPFO	EC_PROCHOT
GPF1	CHG_R_LED
GPF2	CHG_B_LED
GPF3	PWR_LED
GPF4	TP_CLK
GPF5	TP_DATA
GPF6	EC_PECI
GPF7	PM_SYSRST#
GPH0	PWR_KEEP
GPH1	ME_LOCK
GPH2	USB0_EN#
GPH3	PCH_SPI_CS#
GPH4	PCH_SPI_CLK
GPH5	PCH_SPI_SO
GPH6	PCH_SPI_SI
GPG0	EC_BL_EN
GPG1	+3.3VS_ON
GPG2	FLFRAME#
GPG6	LID#
ADC0/GPI0	BATT_TEMP
ADC1/GPI1	ADAPTOR_I
ADC2/GPI2	BAT_I
ADC3/GPI3	BAT_V
ADC4/GPI4	Button3
ADC5/GPI5	PM_SLP_S4#
ADC6/GPI6	PM_SLP_S3#
ADC7/GPI7	SUB_PWR_ACK
	SATA_ODD_DA#_EC
EC_Select	

ITE8518 GPIO Pin Definition List	
DAC0/GPJ0	Fast-charge-EN
DAC0/GPJ1	CHG_ON
DAC0/GPJ2	FAN_CTRL0
DAC0/GPJ3	CHG_I
DAC0/GPJ4	MMB_RESET#
DAC0/GPJ5	SET_V

ITE8518 KB Matrkl interface	
KS10/STB#	KB_SIN0
KS11/AFD#	KB_SIN1
KS12/INIT#	KB_SIN2
KS13/LIN#	KB_SIN3
KS14	KB_SIN4
KS15	KB_SIN5
KS16	KB_SIN6
KS17	KB_SIN7
KS00/PD0	KB_SOUT0
KS01/PD1	KB_SOUT1
KS02/PD2	KB_SOUT2
KS03/PD3	KB_SOUT3
KS04/PD4	KB_SOUT4
KS05/PD5	KB_SOUT5
KS06/PD6	KB_SOUT6
KS07/PD7	KB_SOUT7
KS08/ACK#	KB_SOUT8
KS09/BUSY	KB_SOUT9
KS010/PE	KB_SOUT10
KS011/ERR#	KB_SOUT11
KS012/SLCT	KB_SOUT12
KS013	KB_SOUT13
KS014	KB_SOUT14
KS015	KB_SOUT15

ITE8518 SPI Flash ROM interface	
FSCE0#/GPG2	FLFRAME#
FSCE#	EC_SPI_CS#
FMOSI	EC_SPI_SI
FMOSO	EC_SPI_SO
DSR0#/GPG6	LID#
FSCK	EC_SPI_CLK
SCI#/GPG0	EC_BL_EN

ITE8518 System & LPC Bus	
LAD0	LPC_AD0
LAD1	LPC_AD1
LAD2	LPC_AD2
LAD3	LPC_AD3
SERIRQ	INT_SERIRQ
LFRAME#	LPC_FRAME#
LPCCCLK	CLK_PCI_KBC
WRST#	LRST1#

ITE8518 Clock	
CLK32K	EC32KI
CK32KE	EC32KO

ITE8518 Power	
VSTBY	+3.3VA
VBAT	+3.3VA_RTC
AVCC	+3.3VA
VCC	+3.3V

ITE8518 GND	
AVSS	GND
VSS	GND

Gantiga TDP				
	CPU Socket P	GMCH GFX Freq/Core Volt	Memory	TDP
Gantiga	Penryn SV/FSB800	800MHZ/1.05V	DDR3-1066/ 2 CH	12.0W
Gantiga	Penryn SV/FSB800	800MHZ/1.05V	DDR3-1066/ 2 CH	12.0W
Gantiga	Penryn LV/FSB800	800MHZ/1.05V	DDR3-800/ 2 CH	10.5W
Gantiga	Penryn ULV/FSB800	800MHZ/1.05V	DDR3-800/ 2 CH	9.5W

Ivy Bridge CPU IMVP-7.0			
Voltage (V)	Current (mA)	Measure	Watt
+VCC_CORE	55000		
+VCC_GFXCORE	46000		
+1.05V_VCCP	8500		
+0.85V	6000		
+1.5VS	5000		
+1.8V	1200		

Panther Point PCH			
Voltage (V)	Current (mA)	Measure	Watt
+1.05V_VCCP	43		
+1.05V	5565		
+1.8V	250		
+3.3VS	129		
+3.3V	260		
+5VA	1		
+5V	1		

Cantiga			
VCC	ICC (mA)	W	TEMP (C)
+3.3VS	269	0.887	105
+1.8V	192	0.345	
+1.5VS	76	1.14	
+1.05VS	6013	6.313	
GFX_CORE	6326	6.642	

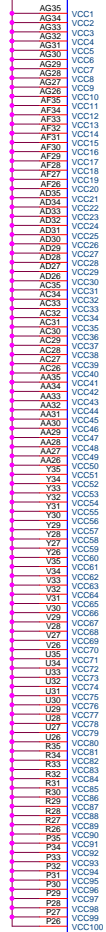
PCH			
VCC	ICC (mA)	mW	TEMP (C)
+5V	2	10	70
+5VS	2	10	
+3.3VA	162	534.6	
+3.3VS	320	1056	
+1.5VS	2220	3330	
+1.05V	1636	1717.8	

ITE8518			
VCC	ICC (mA)	mW	TEMP (C)
+3.3VA	100	330	70

From 53000mA to 55500mA for 45W

POWER

CPU Core 55500 mA
+VCC_CORE

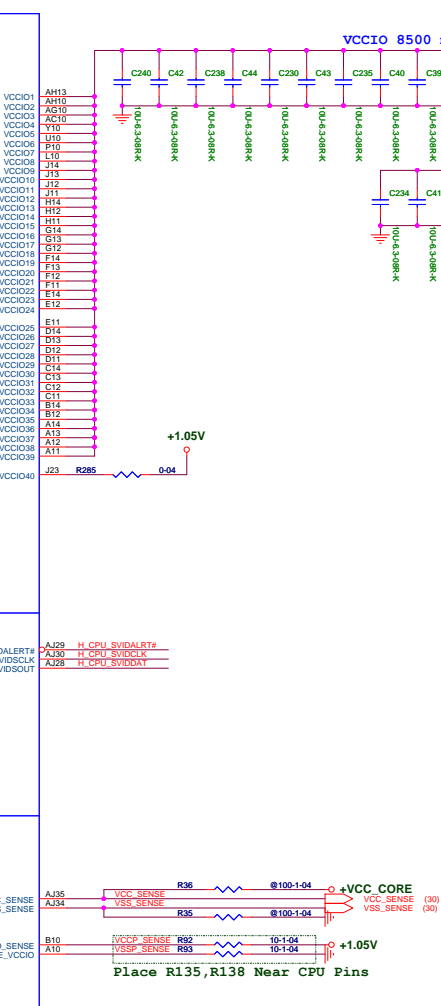


CORE SUPPLY

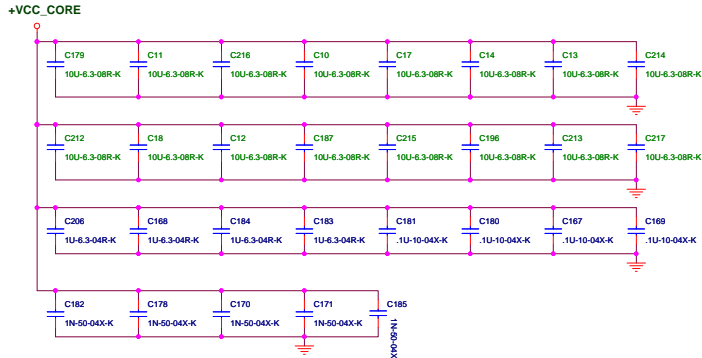
SVID

SENSE LINES

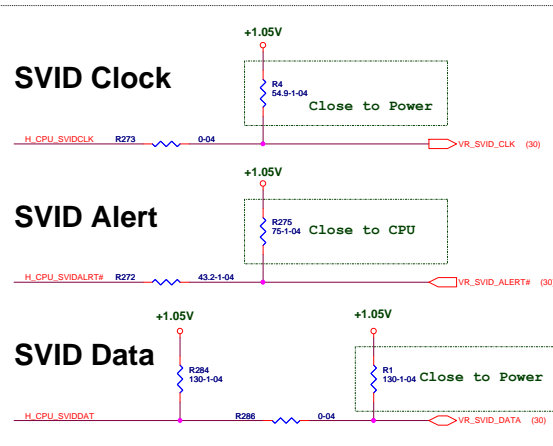
PEG AND DDR



Place R135,R138 Near CPU Pins



CON-CPU-P29821-3622-01H



POWER

GRAPHICS

1.8V RAIL

SA RAIL

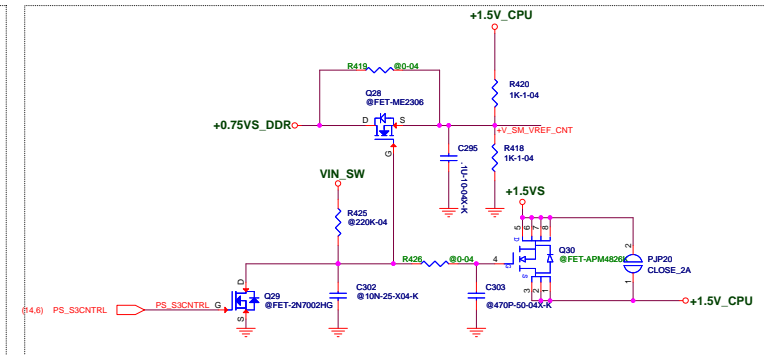
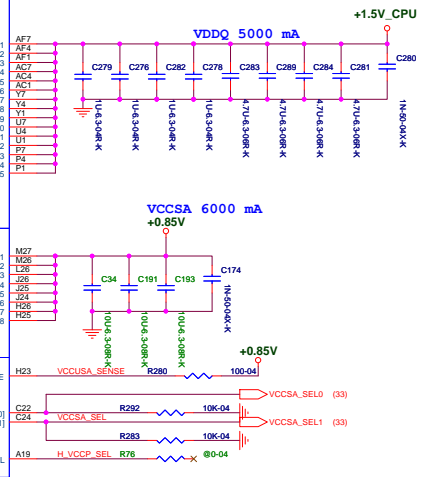
DDR3 - 1.5V RAILS

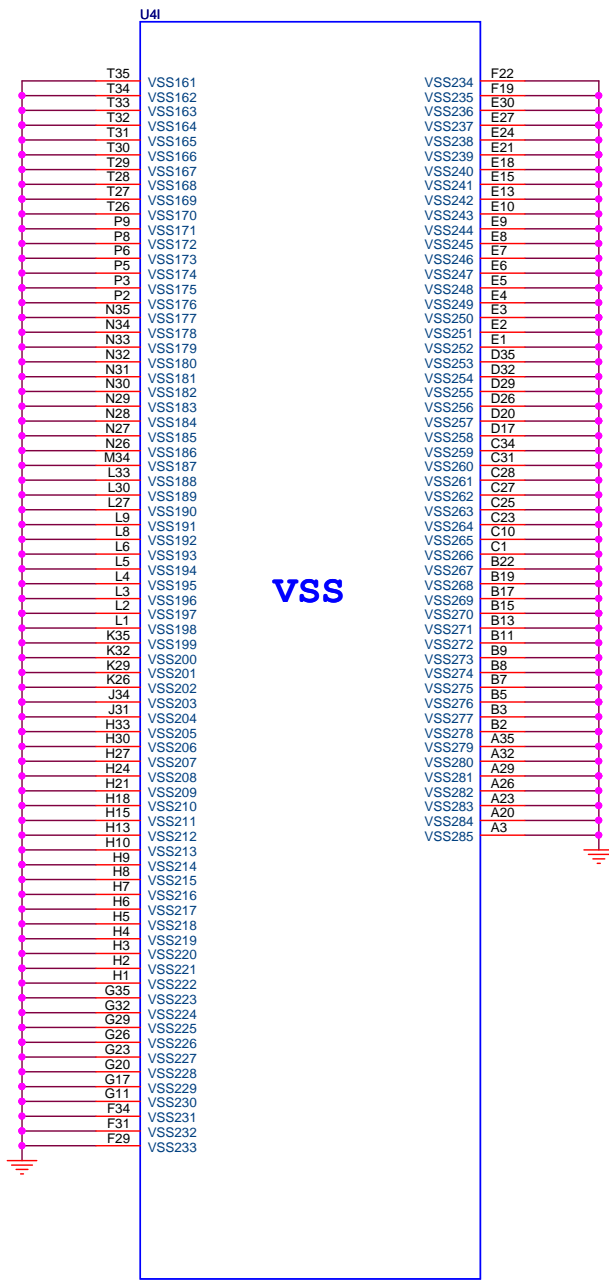
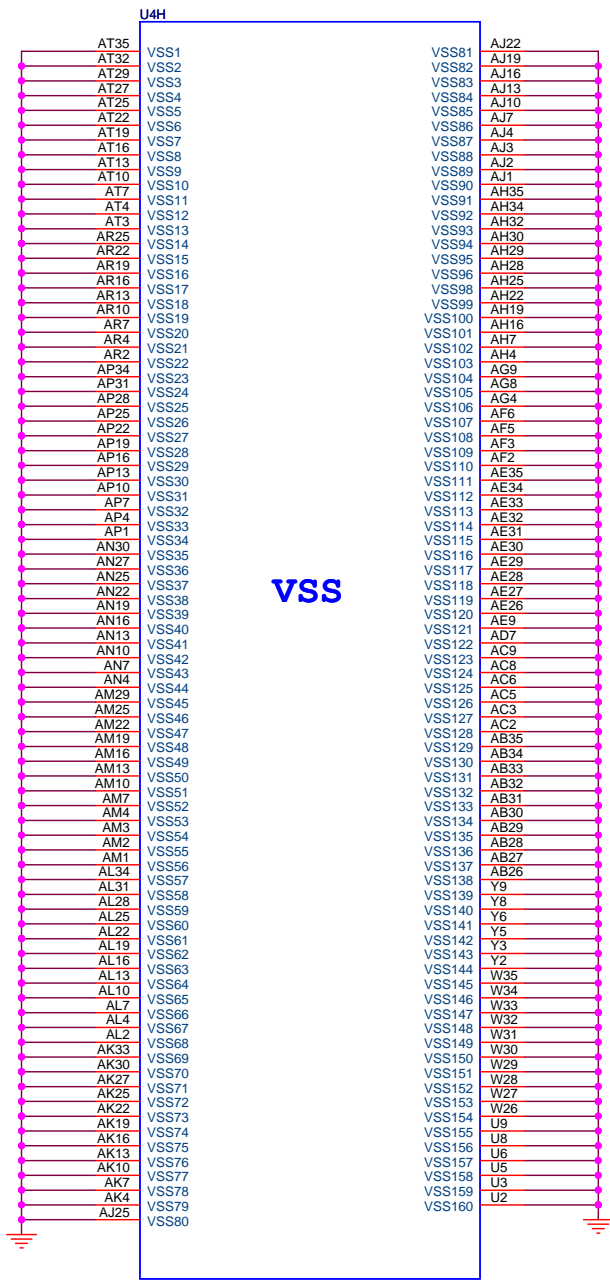
VREF

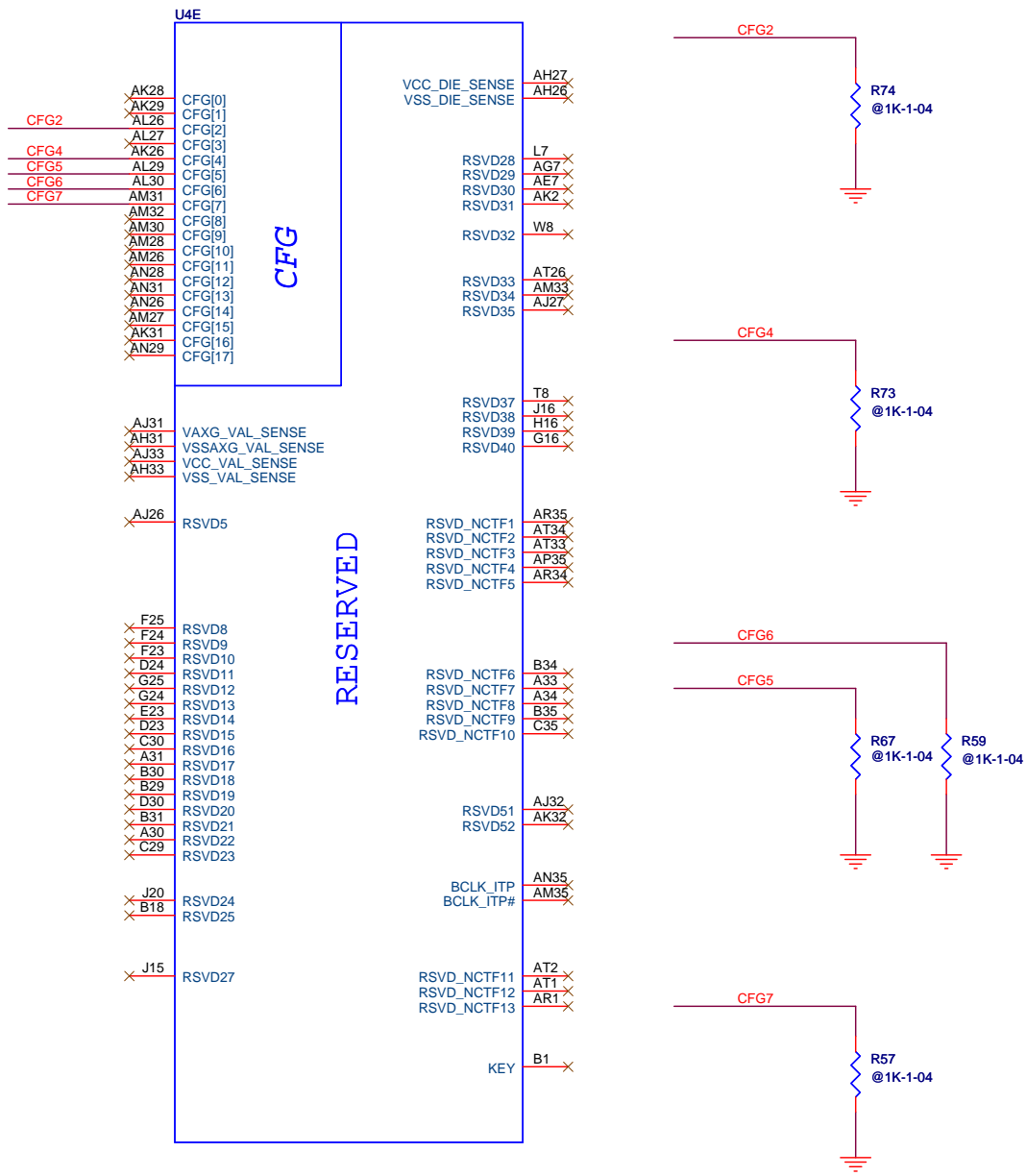
SENSE LINES

When Use UMA R82,R81 Stuff
When Use DGPU Only R82,R81 Unstuff

Note: +V_SM VREF Should
Have 10 mil Trace Width





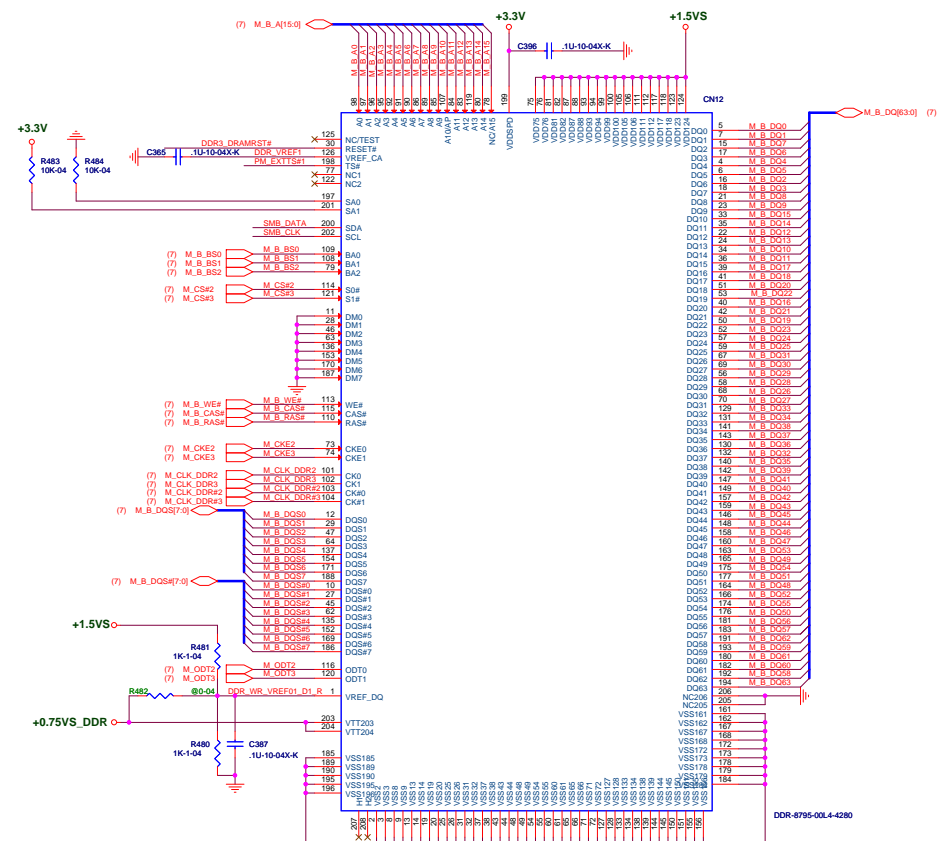
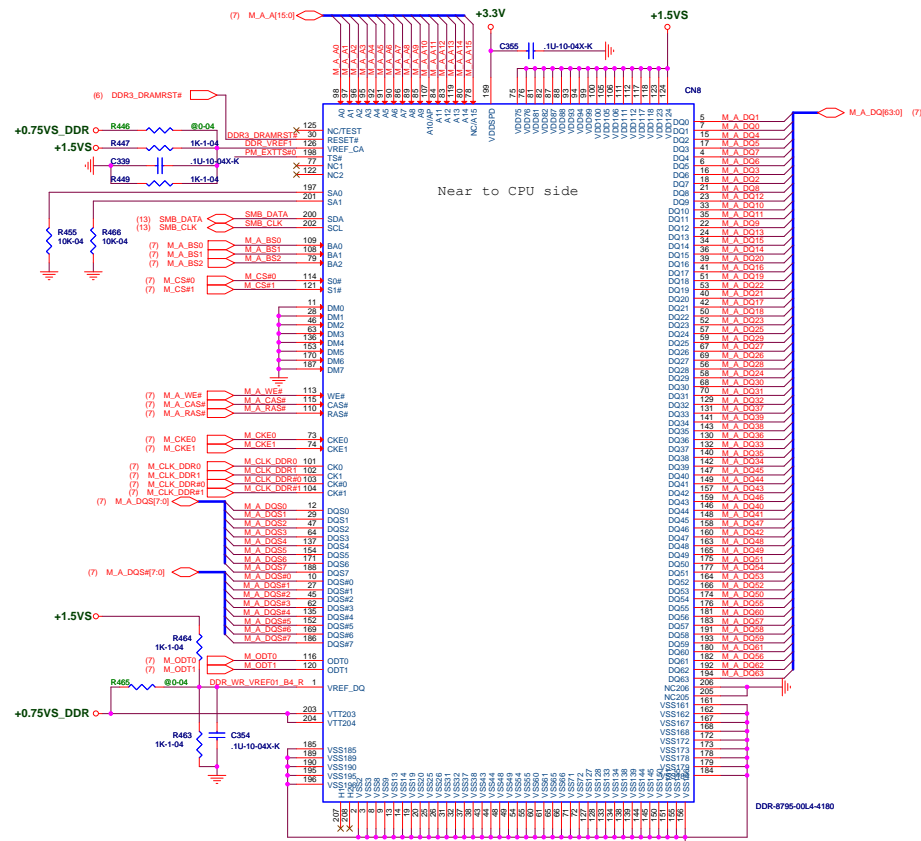


PEG Static Lane Reversal - CFG2 is for the 16x	
CFG2	1:(Default) Normal Operation; Lane # definition matches socket pin map definition 0:Lane Reversed

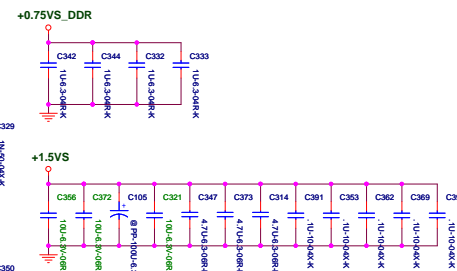
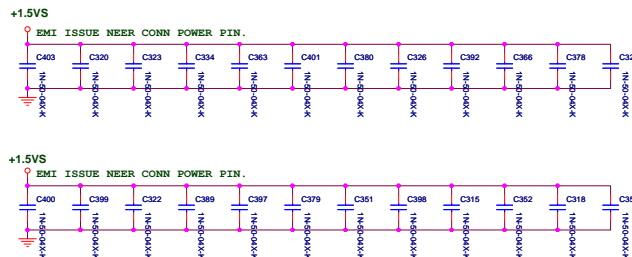
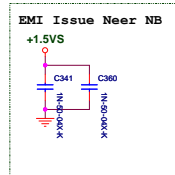
Display Port Presence Strap	
CFG4	1:(Default) Disabled; No Physical Display Port attached to Embedded Display Port 0:Enabled; An external Display Port device is connected to the Embedded Display Port

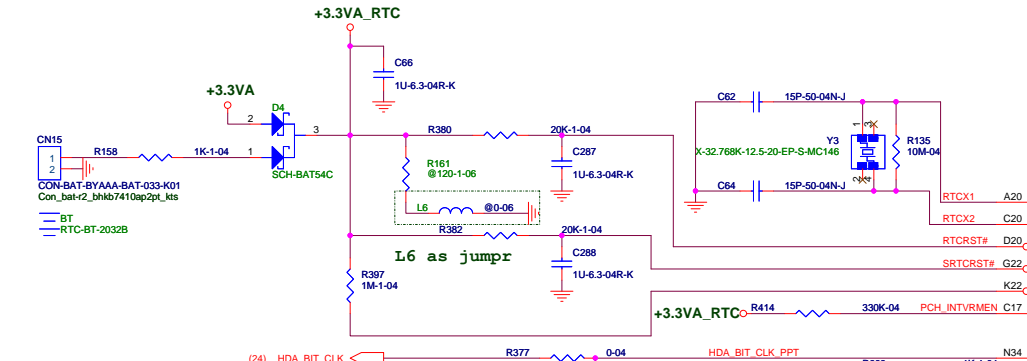
PCIE Port Bifurcation Straps	
CFG[6:5]	11: (Default) x16 - Device 1 functions 1 and 2 disabled 10: x8, x8 - Device 1 function 1 enabled ; function 2 disabled 01: Reserved - (Device 1 function 1 disabled ; function 2 enabled) 00: x8,x4,x4 - Device 1 functions 1 and 2 enabled

PEG DEFER TRAINING	
CFG7	1: (Default) PEG Train immediately following xxRESETB de assertion 0: PEG Wait for BIOS for training

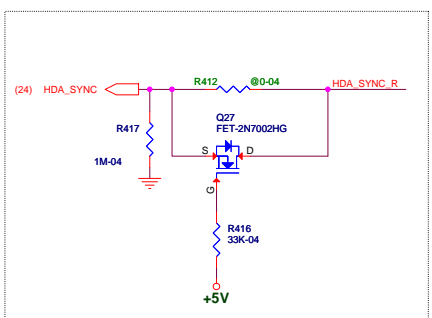
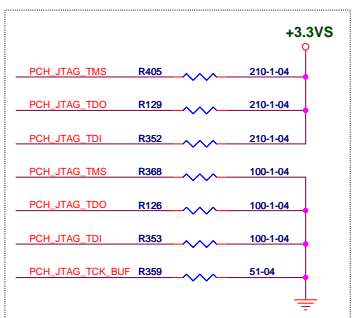


(B) DDR_WR_VREF01_B4 DDR_WR_VREF01_B4 R462 0-04 DDR_WR_VREF01_B4_R
(B) DDR_WR_VREF01_D1 DDR_WR_VREF01_D1 R479 0-04 DDR_WR_VREF01_D1_R

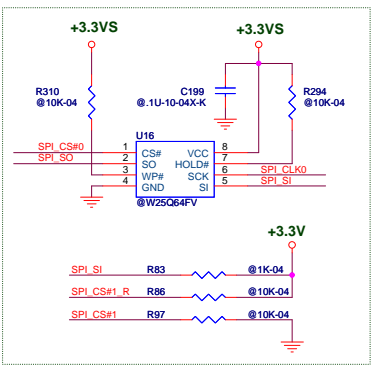
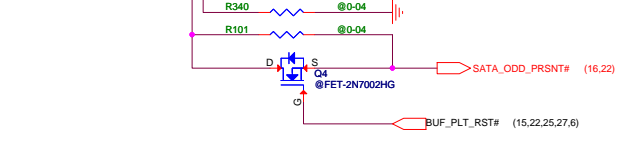
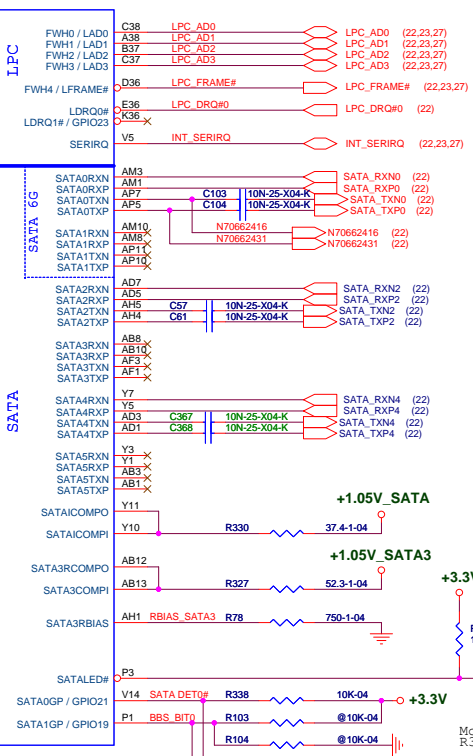
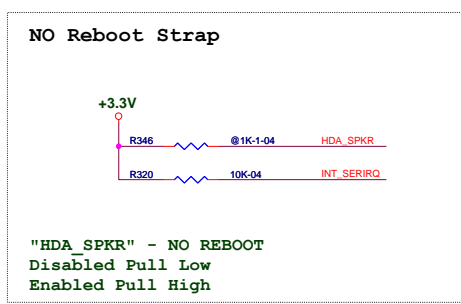
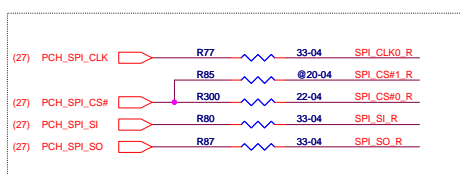
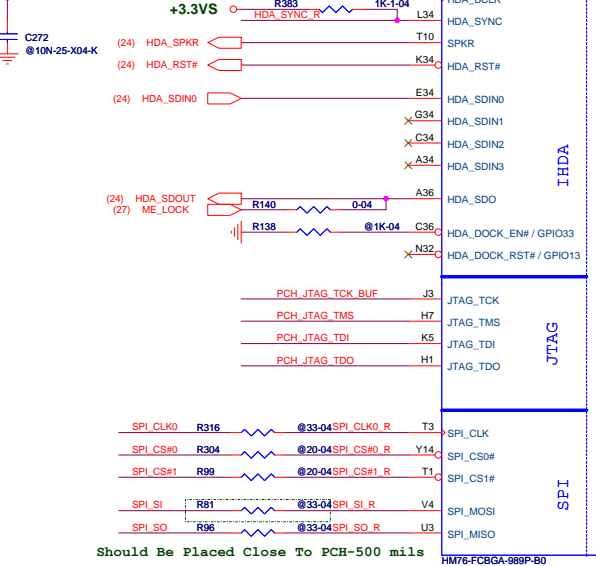




INTVRMEN- Integrated SUS
1.05V VRM Enable
High - Enable Internal VRs
Low - Enable External VRs



Flash Descriptor Security Override	
HDA_SDOUT	Low = Disabled - Default High = Enabled



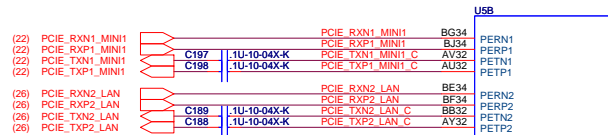
SATA Ports Table

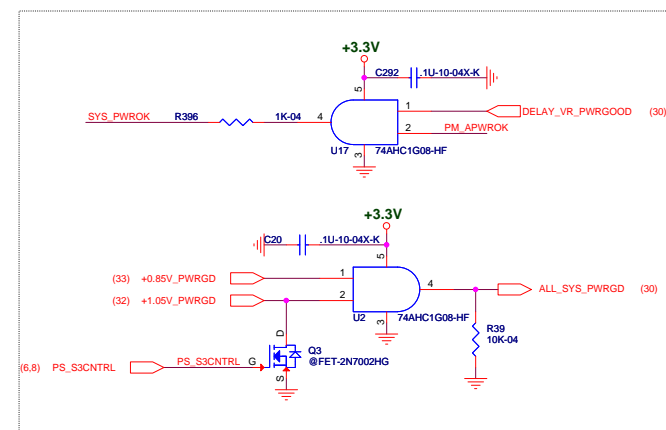
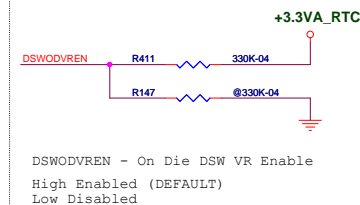
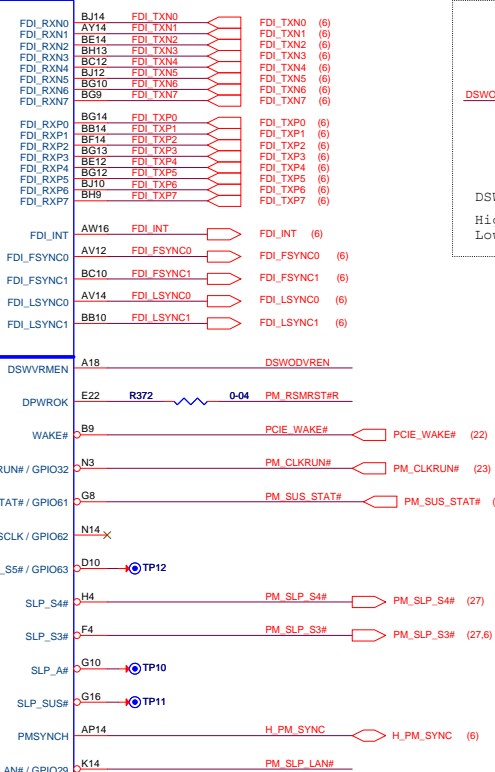
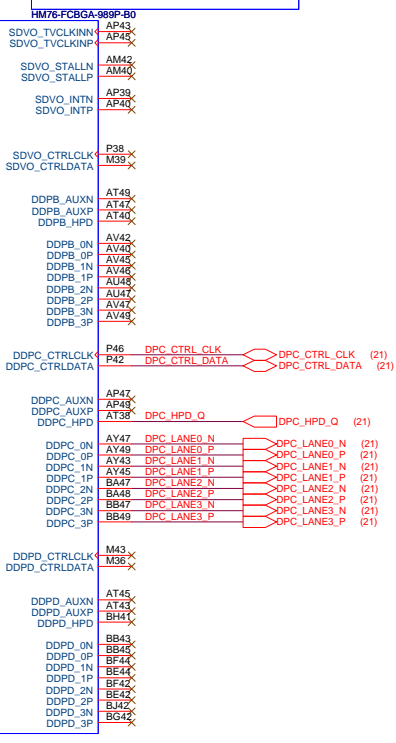
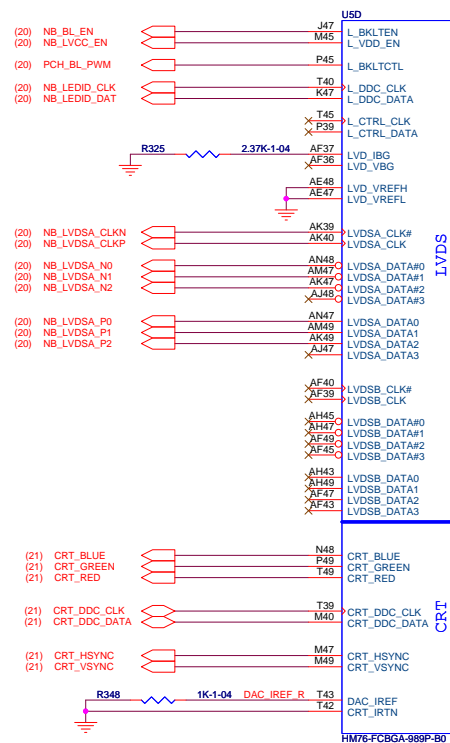
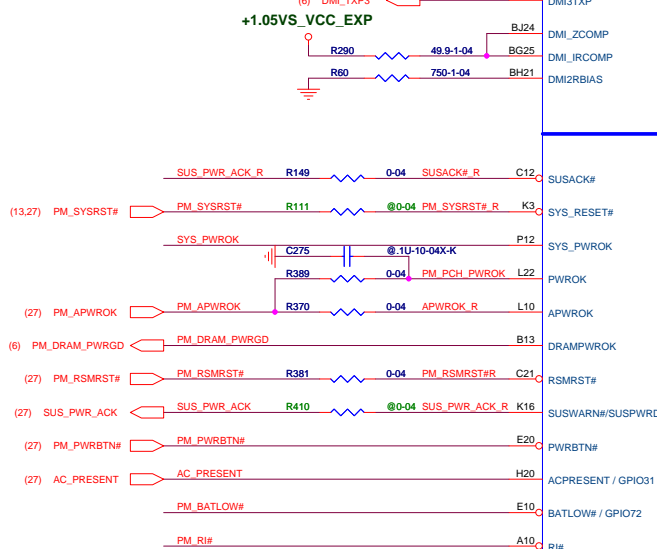
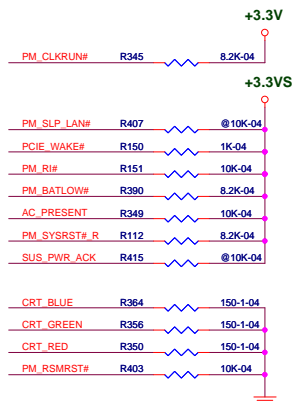
SATAN0	SATA P0	HDD 6G
SATAN1	SATA P1	Empty(HM70 Disable)
SATAN2	SATA P2	ODD
SATAN3	SATA P3	Empty(HM70 Disable)
SATAN4	SATA P4	M-SATA(Optional)
SATAN5	SATA P5	None(HM70)

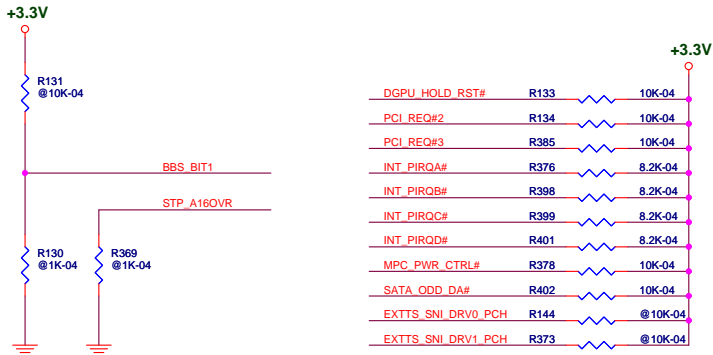
2012-3-13
recovery

Modify 3/29
R336.1 of net name "SATA_LED#" change to "SATA_LED2#"

Modify 3/12
U16 package change from M-SO8 to sop8-5_3x5_3x2_2



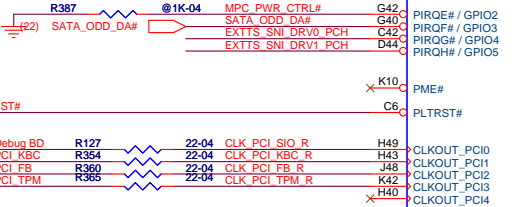
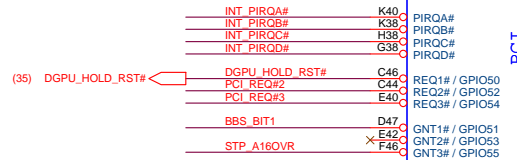
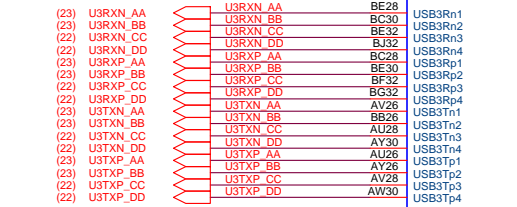
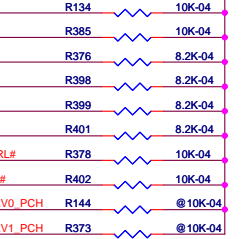




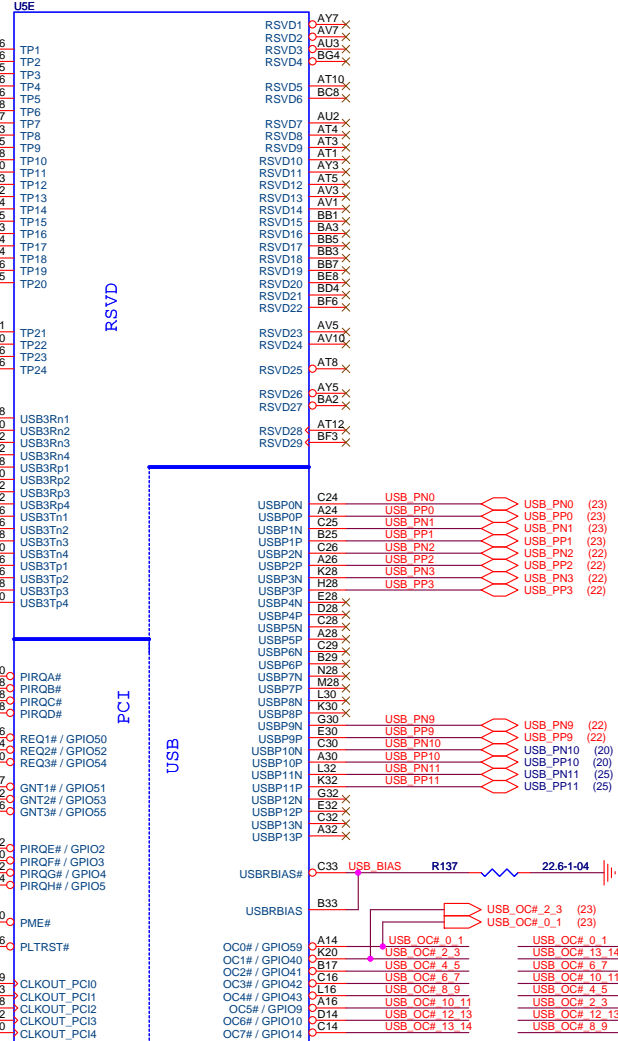
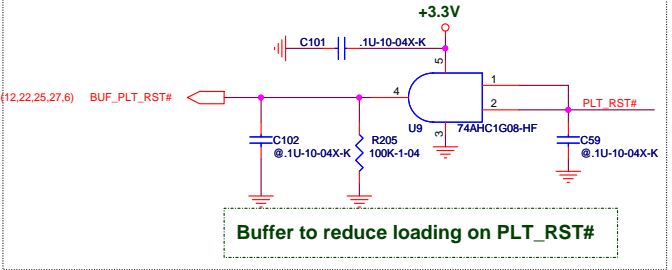
Boot BIOS Strap		
BBS_BIT1	BBS_BIT0	Boot BIOS Location
0	0	LPC
0	1	Reserved (NAND)
1	0	-
1	1	SPI

A16 swap override Strap	
STP_A16OVR	LOW = A16 swap override High = Default

MPC Switch Control
MPC OFF -- (1-X) [Default]
MPC ON -- (1-2)

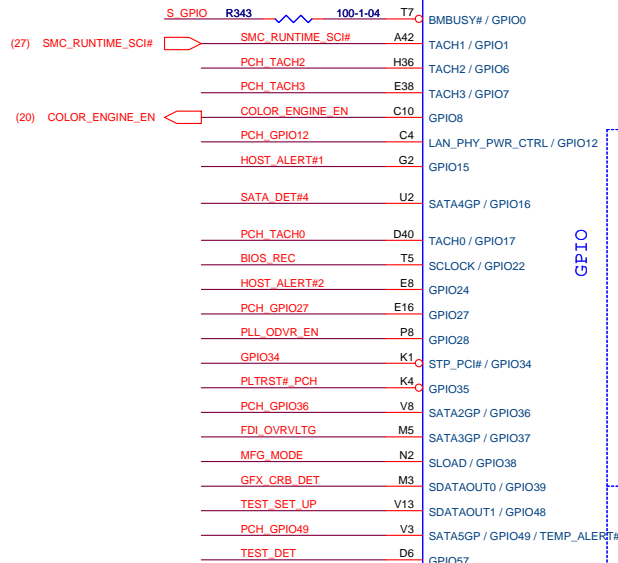
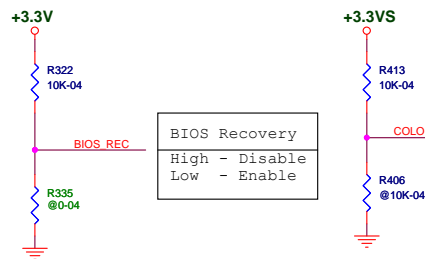
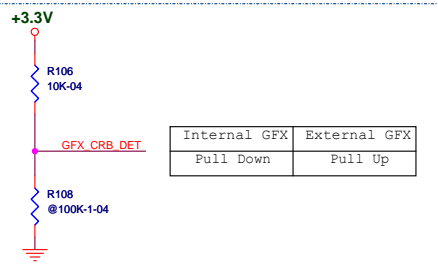
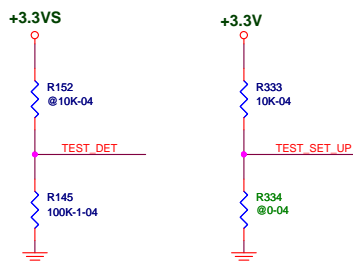
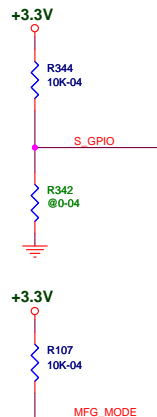


TPM Function Select	
W/TPM	R365 Unstuff
W/O TPM	R365 Stuff



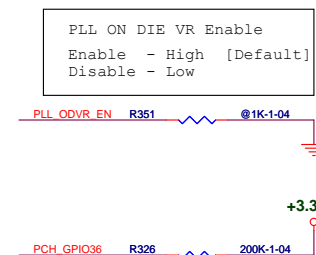
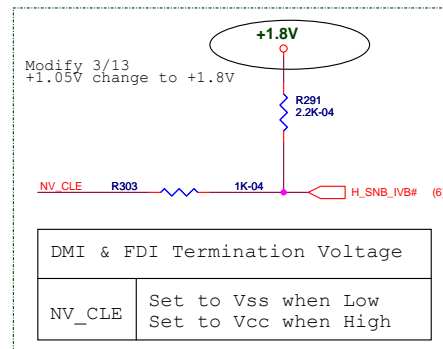
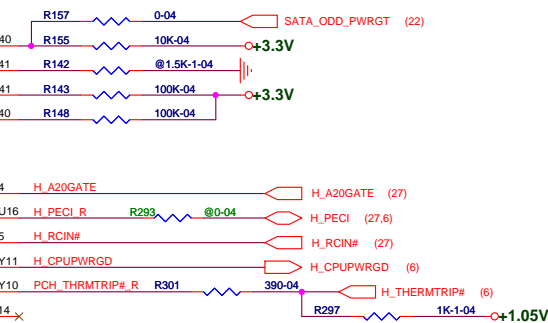
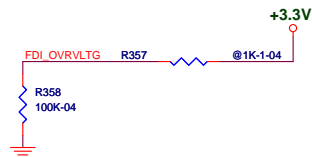
USB Ports Table	
USBP0	Enhance USB3.0 USB_0
USBP1	Enhance USB3.0 USB_1
USBP2	Enhance USB3.0 USB_2 (DB)
USBP3	Enhance USB3.0 USB_3 (DB)
USBP4	Empty
USBP5	Empty
USBP6	Empty
USBP7	Empty
USBP8	Empty
USBP9	WLAN / BT USB_9
USBP10	Web Camera USB_10
USBP11	Card Reader USB_11 (MB)
USBP12	Empty
USBP13	Empty

(12,22) SATA_ODD_PRSENT# R329 0-04 PCH_GPIO36

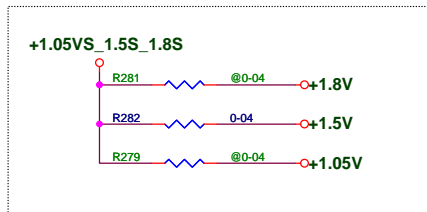
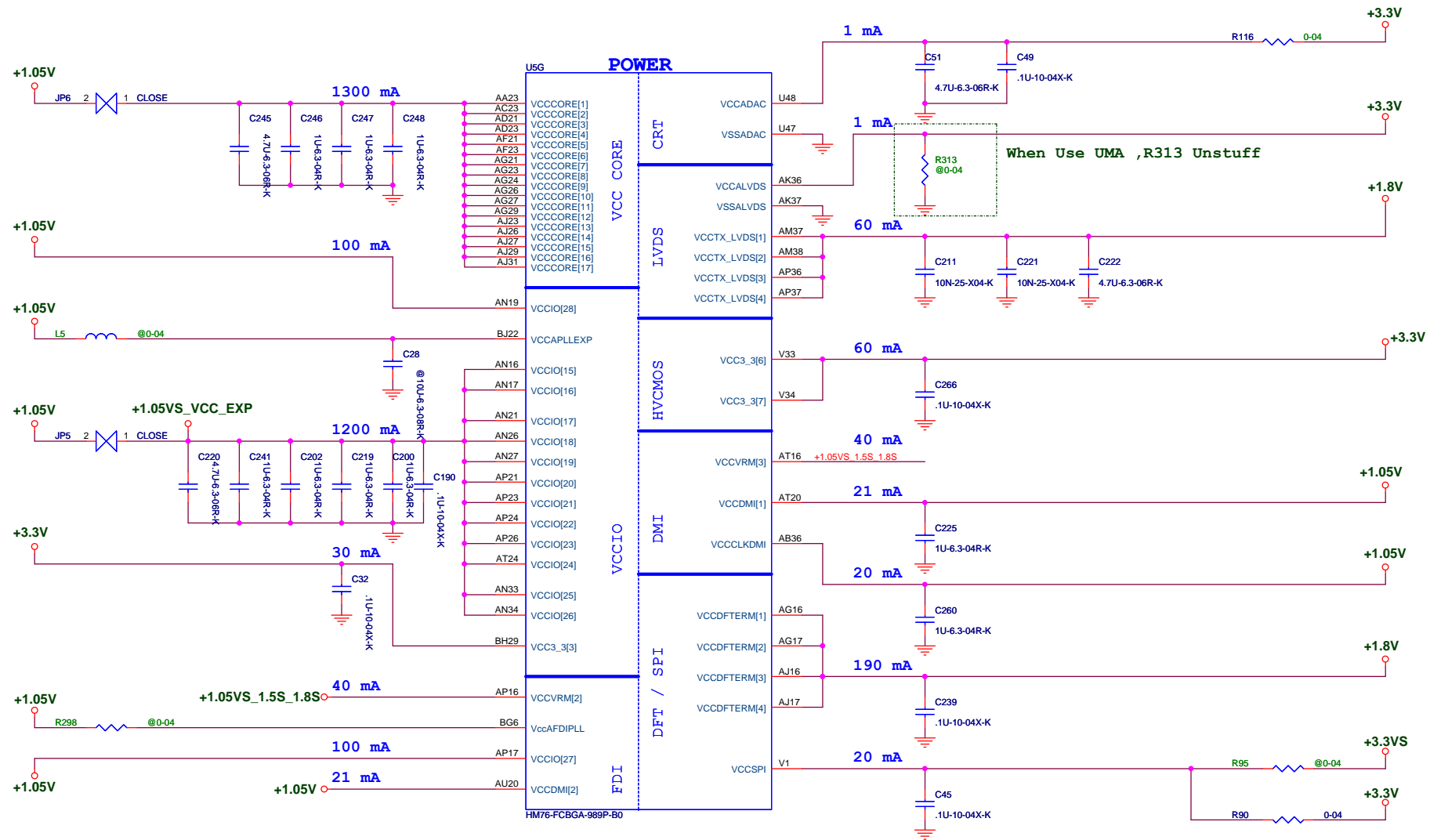


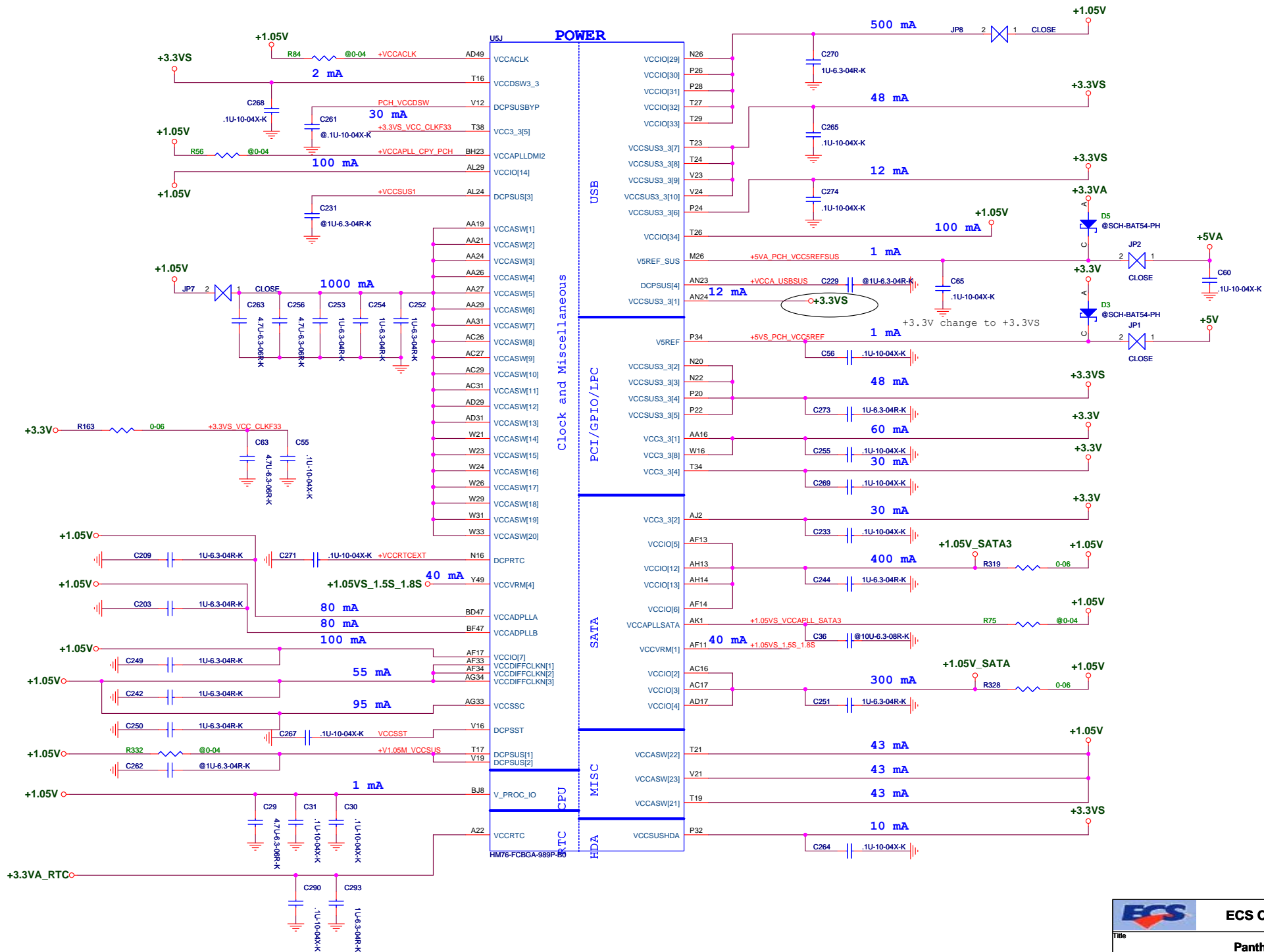
GPIO

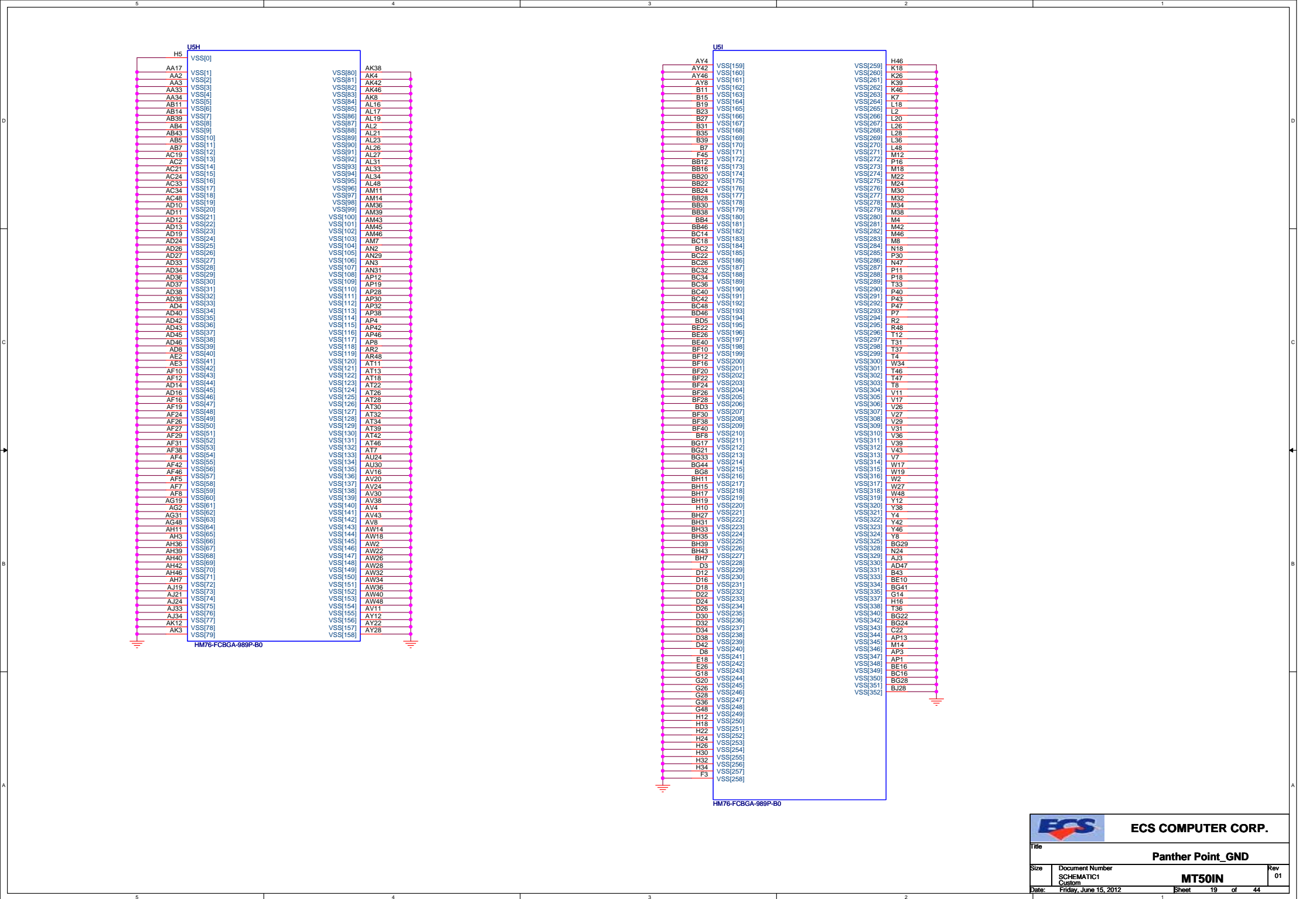
NCTF



FDI TERMINATION VOLTAGE OVERRIDE		DMI TERMINATION VOLTAGE OVERRIDE	
GPIO37 (FDI_OVRVLTG)	LOW - Tx, Rx terminated to same voltage (DC Coupling Mode) DEFAULT	GPIO36 (SATA_ODD_PRSENT#)	LOW - Tx, Rx terminated to same voltage (DC Coupling Mode) DEFAULT

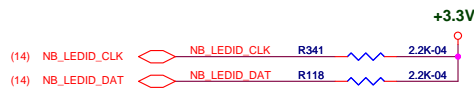




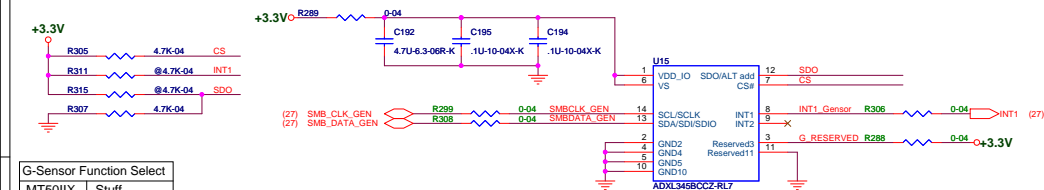


[illegible]

CN1 footprint is from con_wb-10v100_jh3-2232-103n_fcn to con_wb-10v100_a1001wv-sf-2x_hr for ME request

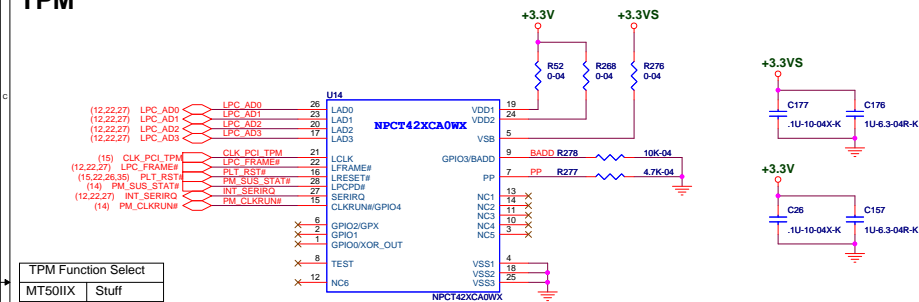


D G-Sensor



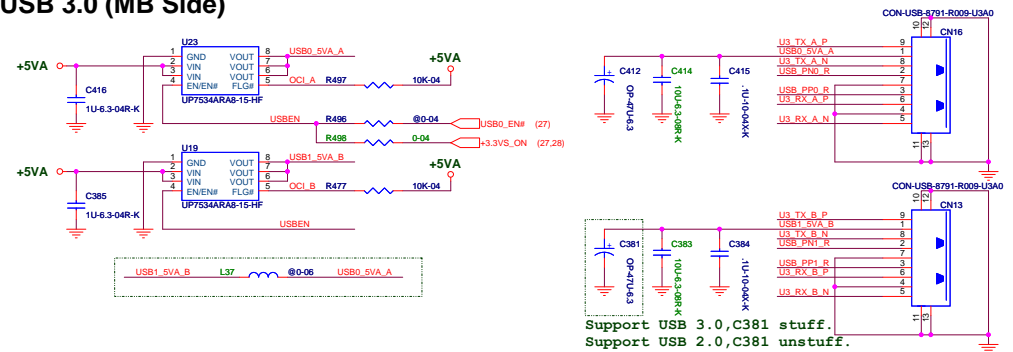
G-Sensor Function Select	
MT50IIX	Stuff
MT50INX	Stuff

TPM



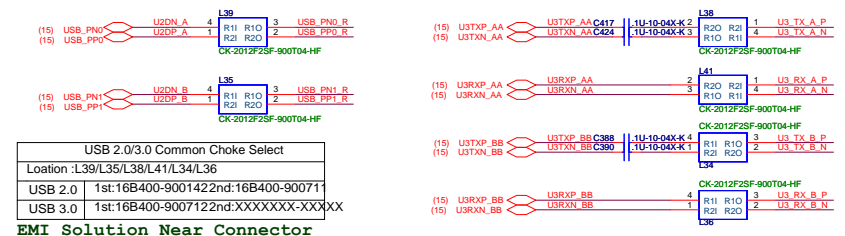
TPM Function Select	
MT50IIX	Stuff
MT50INX	Stuff

USB 3.0 (MB Side)

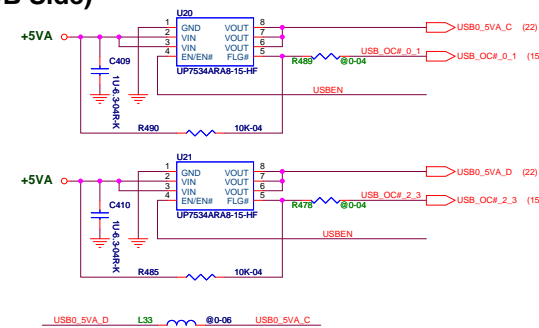


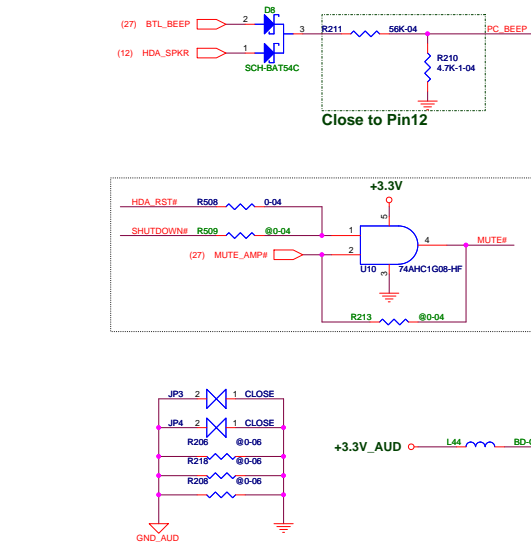
EMI Issue

PCH USB 2.0 Port 0 & Port 1 PCH USB 3.0 Port A & Port B



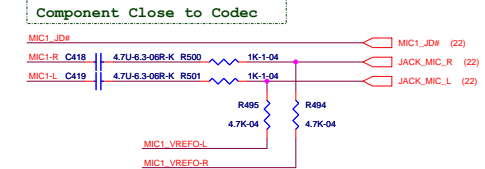
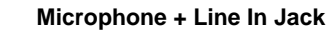
USB 3.0 (DB Side)



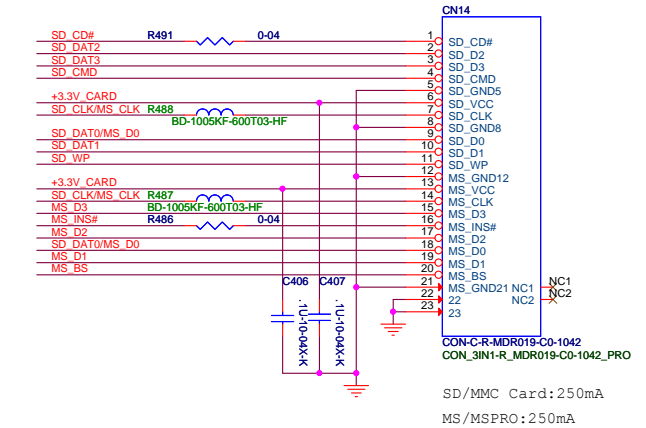
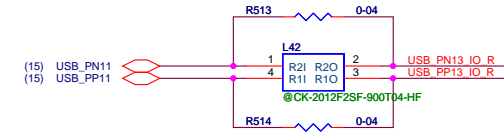
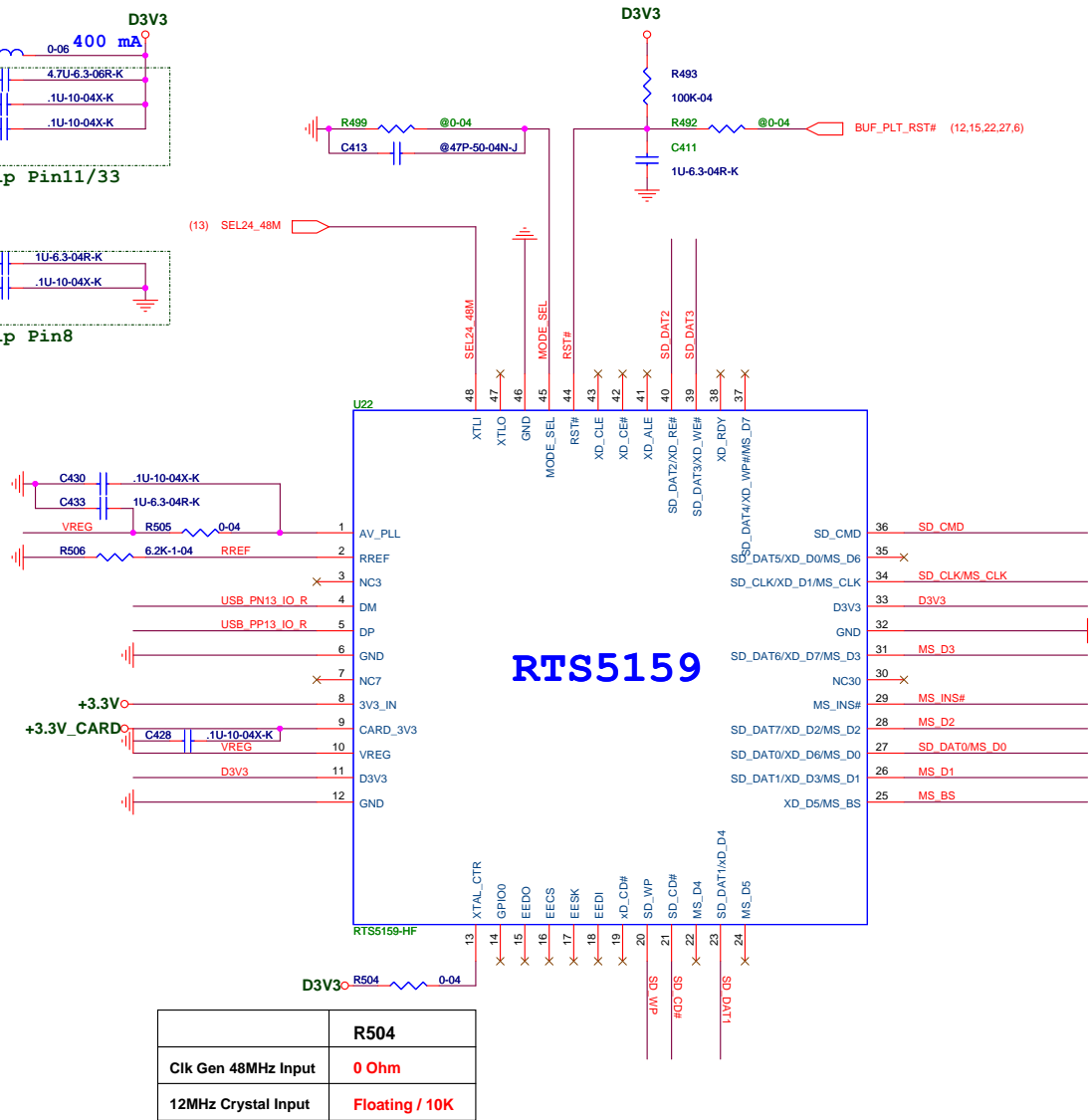
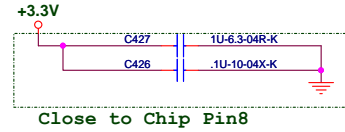
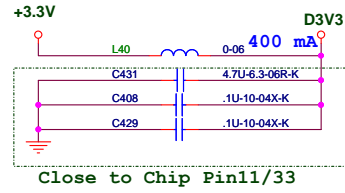


When Use ALC269VB; L21, L20 need stuff ; other unstuff

Speaker Connector

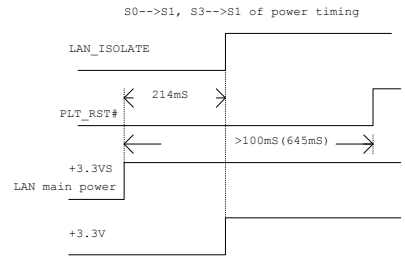
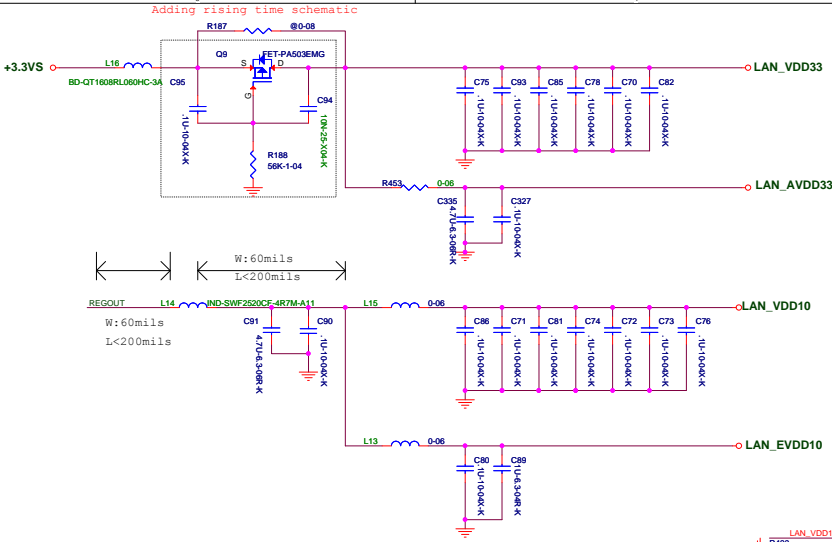


Card Reader



Card Reader Function Select	
MT50IIX	Stuff
MT50INX	Stuff

ECS COMPUTER CORP.	
Title	
Card Reader (RTS5159-GR)	
Size	Document Number
MT50IN	SCHEMATIC1
Date:	Friday, June 15, 2012
Sheet	25 of 44
Rev	01



10/100M and Giga LAN of select table

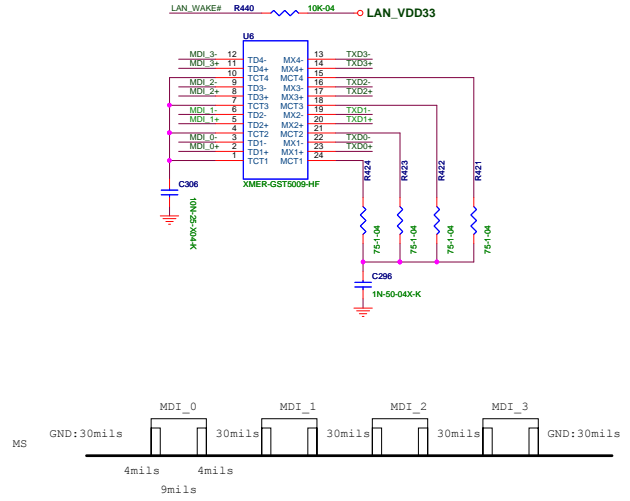
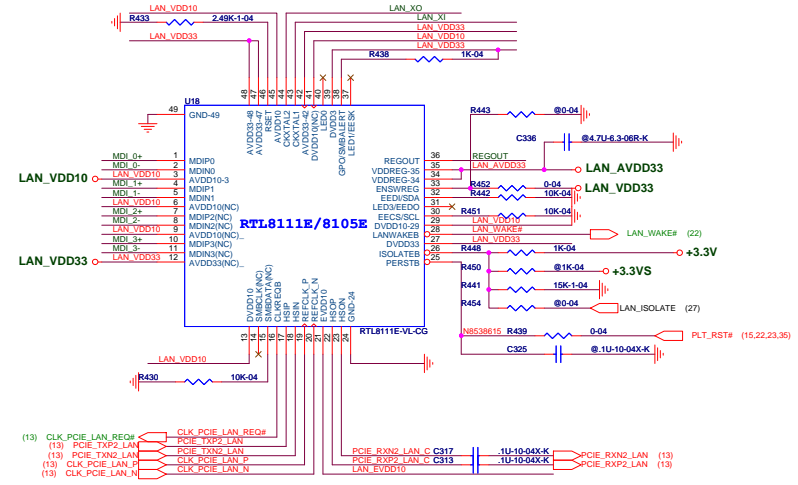
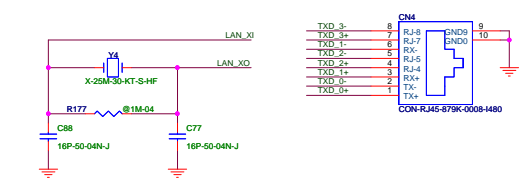
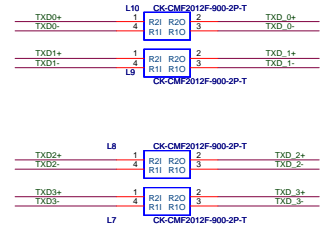
LAN Type	ECS Part Number and Location		PHY Transceiver
	U18	U6	
10/100M	RTL8105E	27A001284-00	XMERTST1284A
Giga LAN	RTL8111E-VB-GR	27A005009-10	XMER-GST5009
Giga LAN	RTL8111E-VL-CGT		

Location Chipset	L14	C91, C90	C335, C327	R453	R452, R430	R443	R441	R421, R422
RT8105	X	X	X	X	X	V	X	V
RTL8111E	V	V	V	V	V	X	V	V

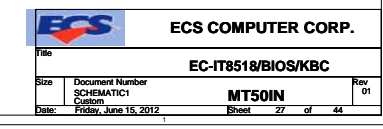
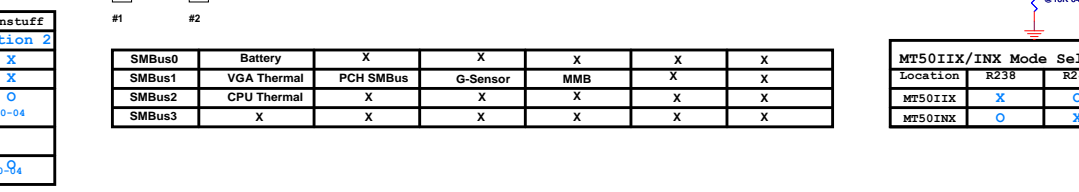
X is show Unstuff
V is show Stuff

Modify 4/10

L10, L9, L8, L7 are from CK-MCM2012B900GBE to CK-CMF2012F-900-2P-T for EMI request



MS is maximum, total widths of space with 2 near to ground is 218mils

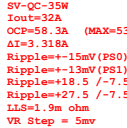


	Configure Phase	Setting Mode
VCC_CORE	2 Phase	PWM3 pin connect to +5V
	1 Phase	PWM3 and ISEN2 pin connect to +5V
GFX_CORE	1 Phase	ISUMNG pin connect to +5V

Modify 4/5 Adding 6 of capacitor for power request

Frequency Adjust transient waveform for GE

Adding 6 of capacitor for power request

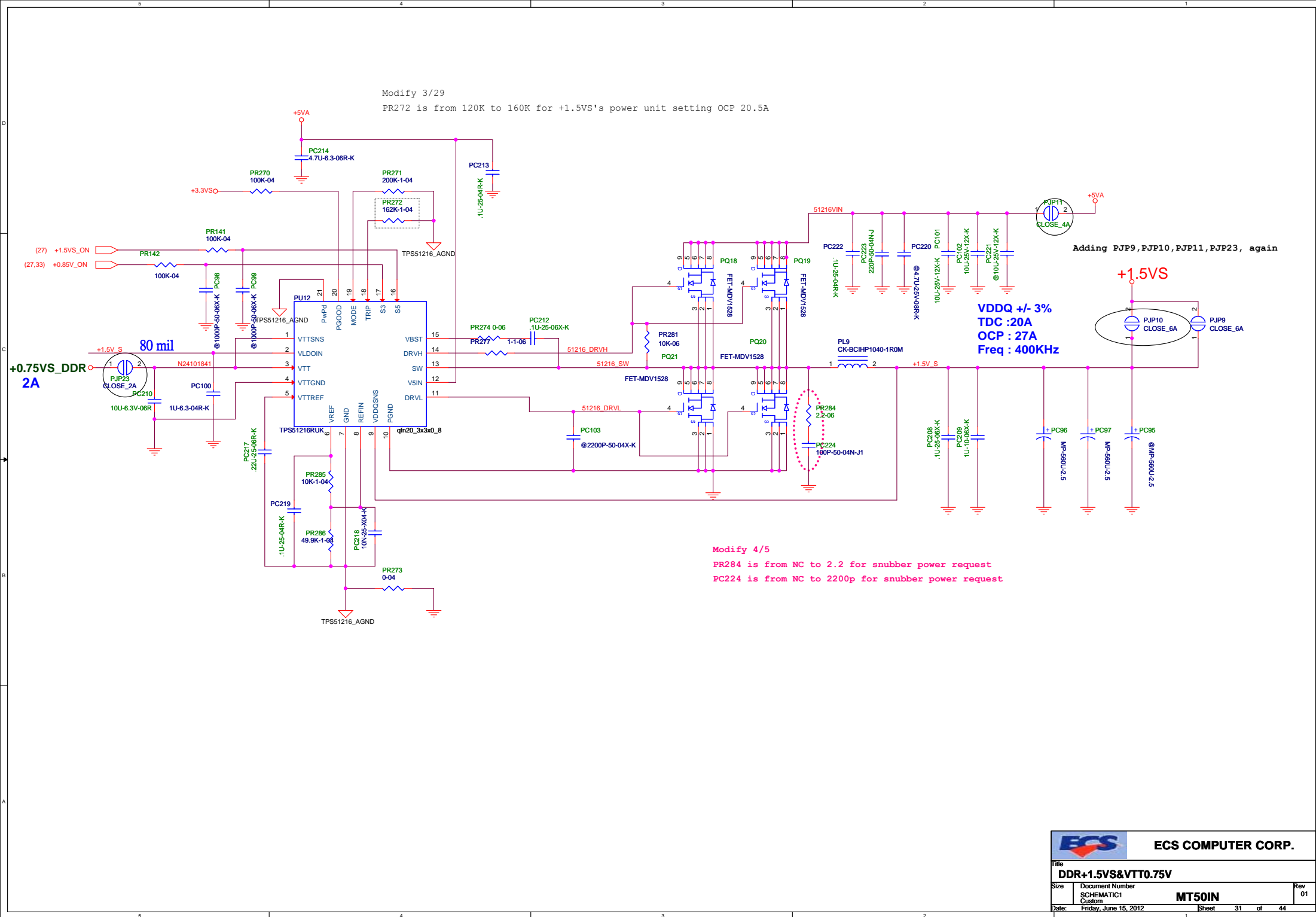


Adding 4 of capacitor for power request

Switch Frequency=300KHz

+VCC_CORE

PC67 are from cap smt 6 3X7 4X5 8 to SCAR250



Modify 4/9
PR18 is from 12.7K(OCP=24A) to 16.5K(OCP=25A)
PC18 is from 3.3n to 8.2n for transient response
PL3 material change is from BC1HP1040-4R7 to TMPC1004H-2R2M-201

Output Voltage = [Vref x R2/(R1+R2)] x 2

Modify 3/29 PR8 is from 26.1K to 24K for enhance +1.05V
PR9 is from 137K to 124K for enhance +1.05V

Modify 4/11
Adding PR289

Output Voltage = [Vref x R2/(R1+R2)] x 2

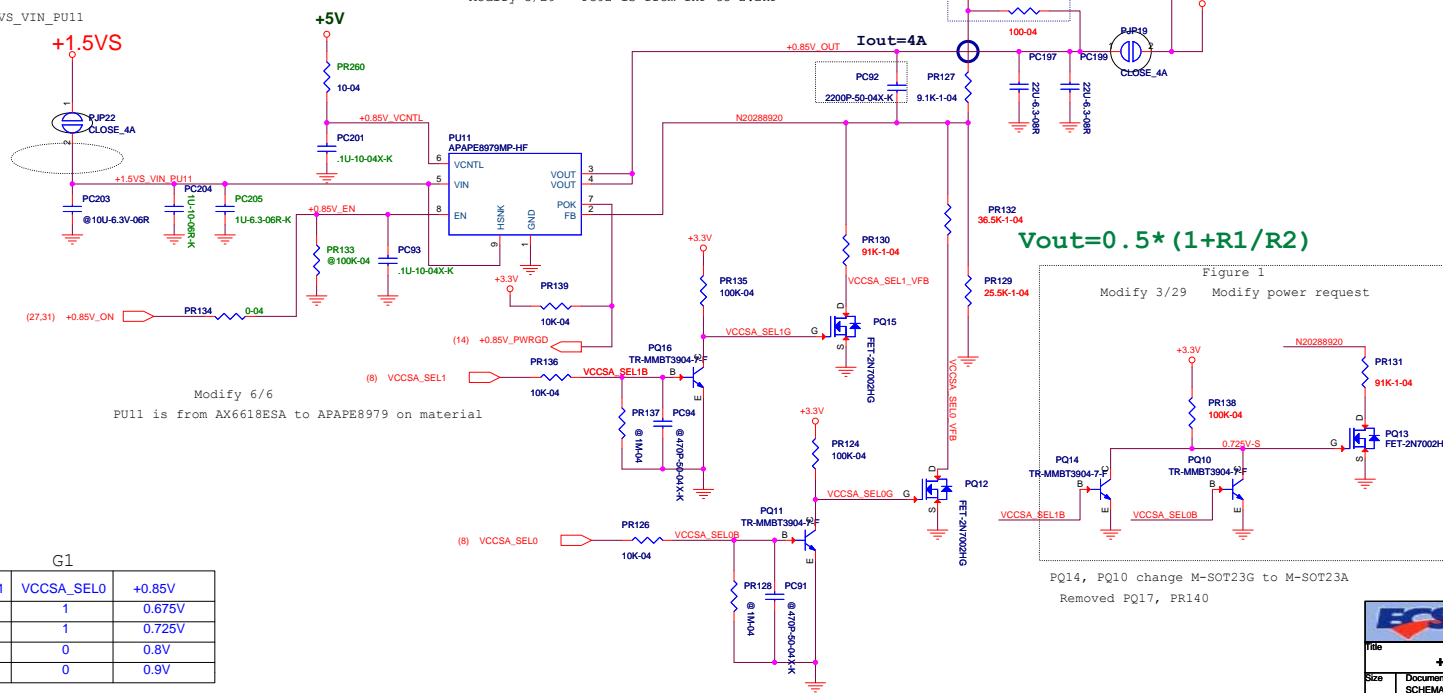
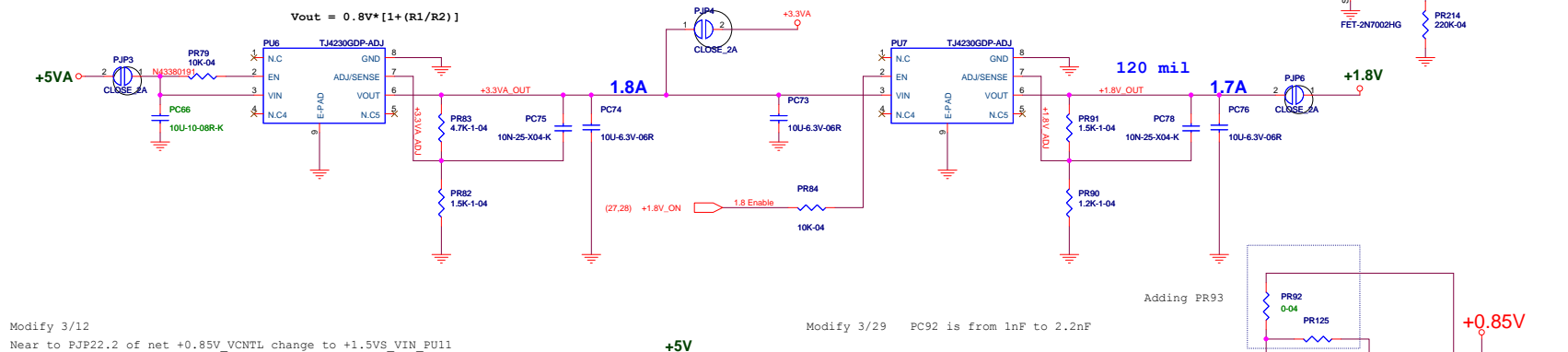
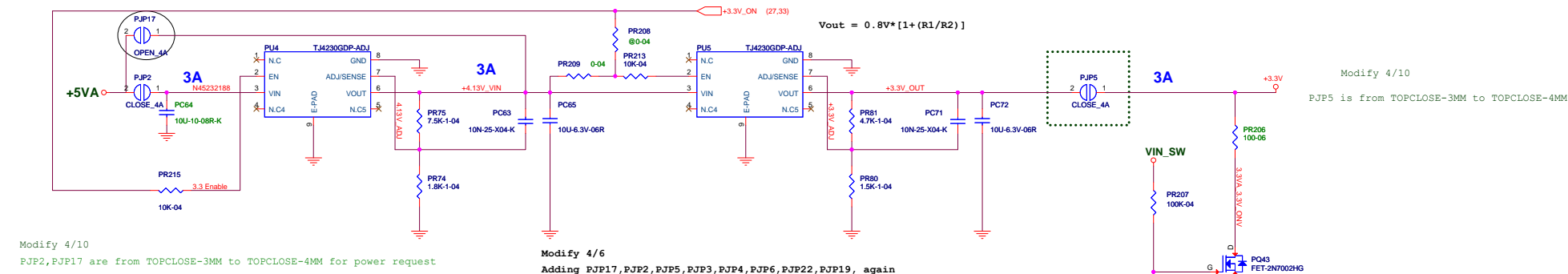
Modify 4/9
PR17 is from 56K(OCP=17.6A) to 33K(OCP=20A)
PC13 is from 3.3n to 8.2n for transient response
PR144 is from 0 to 30K for Tset
PR145 is from NC to 73.2K for Tset

Modify 4/9
Adding PR287
PR287 is close to OZ8153
Adding PC241, PC241

Modify 4/5
PR201, PR195 are from NC to 2.2 for snubber power request
PC142, PC133 are NC to 2200p for snubber power request
Adding PJ1, PJ2, PJP13, PJP14, again

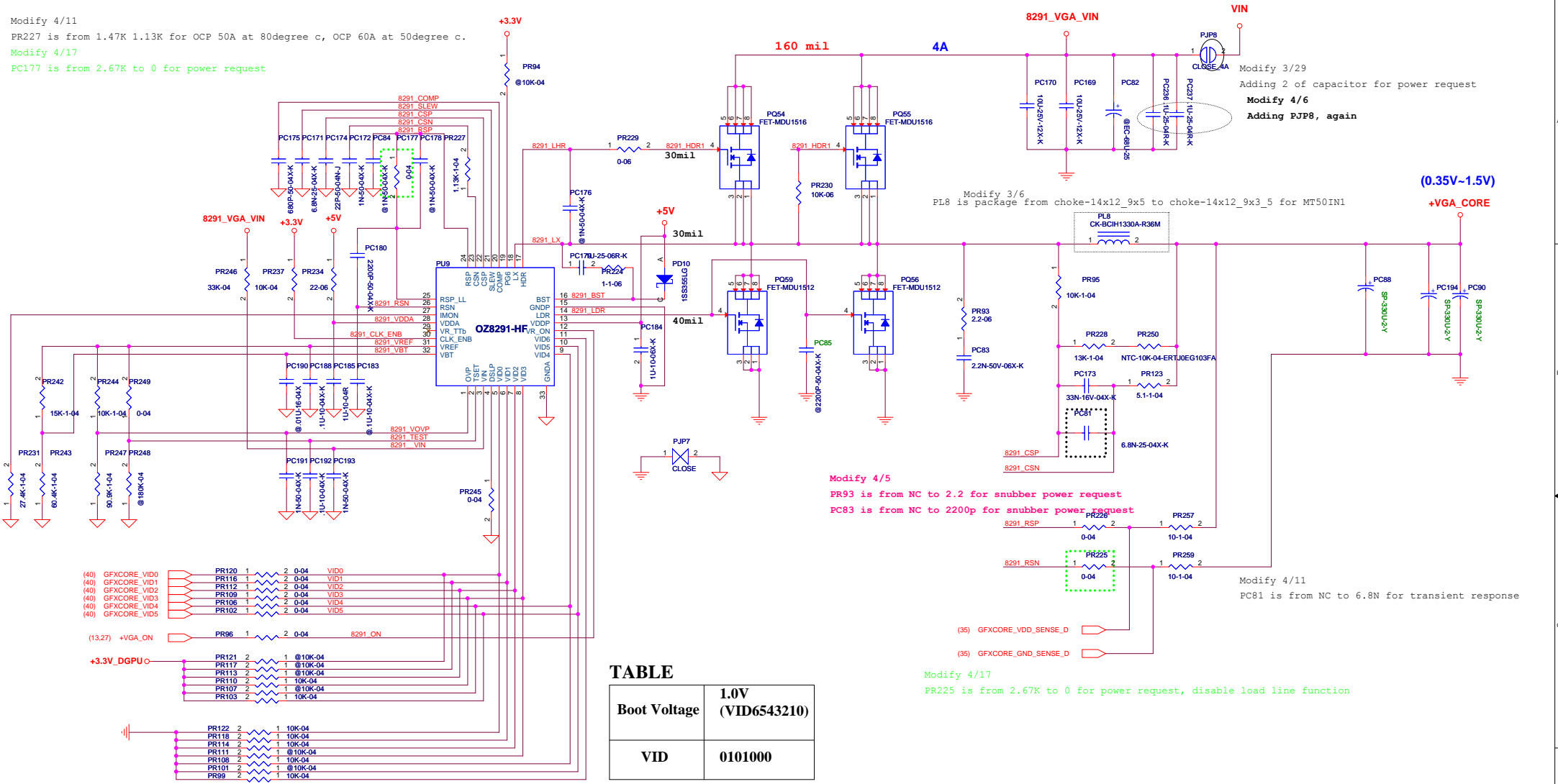
$F = Vset * (Vin/2 - Vset) / (2us * Vtest * Vin/2)$
 $Vset = Vout/2, Vtest = 2.75V$

Modify 4/11
PJP17 is from TOPCLOSE-4MM to TOPOPEN-4MM



G0	G1	
VCCSA_SEL1	VCCSA_SEL0	+0.85V
1	1	0.675V
0	1	0.725V
1	0	0.8V
0	0	0.9V

Modify 4/11
PR227 is from 1.47K 1.13K for OCP 50A at 80degree c, OCP 60A at 50degree c.
Modify 4/17
PC177 is from 2.67K to 0 for power request



Modify 3/6
PL8 is package from choke-14x12_9x5 to choke-14x12_9x3_5 for MT50IN1


Modify 3/29
Adding 2 of capacitor for power request
Modify 4/6
Adding PJP8, again

Modify 4/5
PR93 is from NC to 2.2 for snubber power request
PC83 is from NC to 2200p for snubber power request

Modify 4/11
PC81 is from NC to 6.8N for transient response

Modify 4/17
PR225 is from 2.67K to 0 for power request, disable load line function

+VGA_CORE Select
MT55IIX Unstuff
MT55INX Stuff

**ECS COMPUTER CORP.**

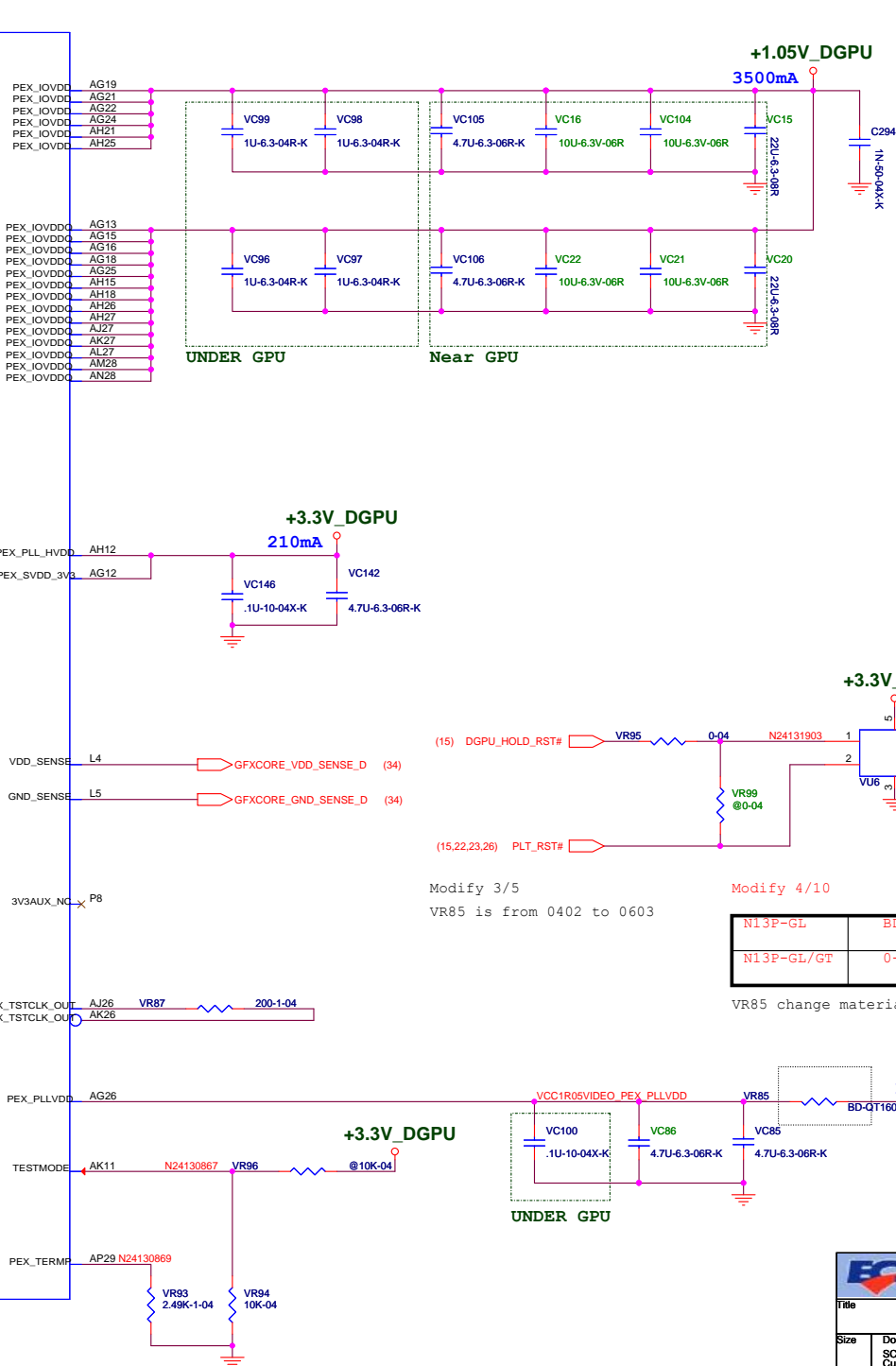
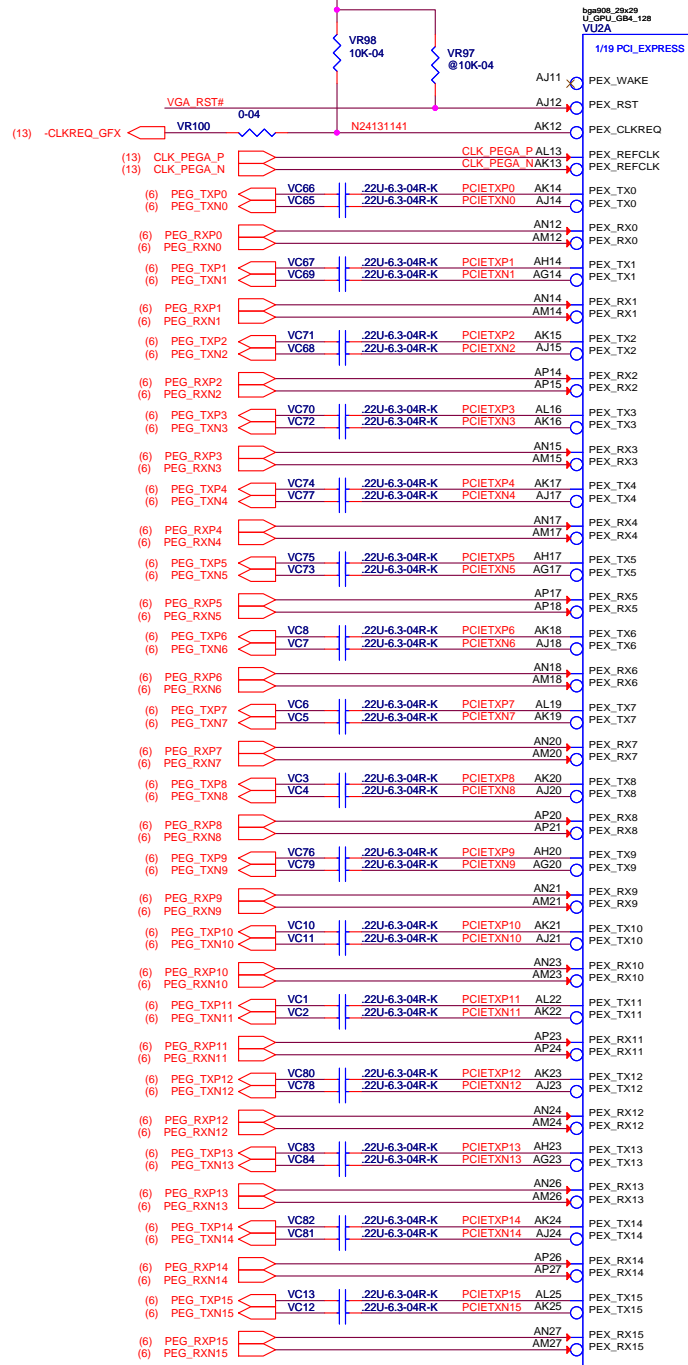
File
VGA_Core (OZ8291)

Size
Document Number
SCHEMATIC1
Rev
01

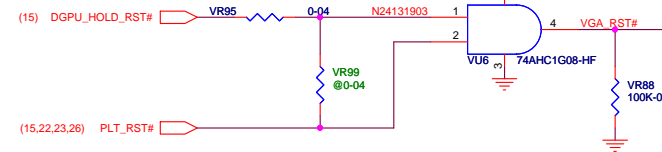
Date
Friday, June 15, 2012
Sheet
34 of 44

MT50IN

+3.3V_DGPU



+3.3V_DGPU



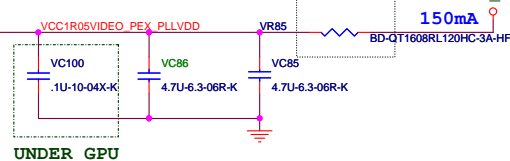
Modify 3/5
VR85 is from 0402 to 0603


Modify 4/10

N13P-GL	BD-QT1608RL120HC-3A-HF
N13P-GL/GT	0-06

VR85 change material

+1.05V_DGPU



**ECS COMPUTER CORP.**

Title

VGA PCIE

Size

Document Number

Rev

SCHEMATIC1

Custom

01

Date:

Friday, June 15, 2012

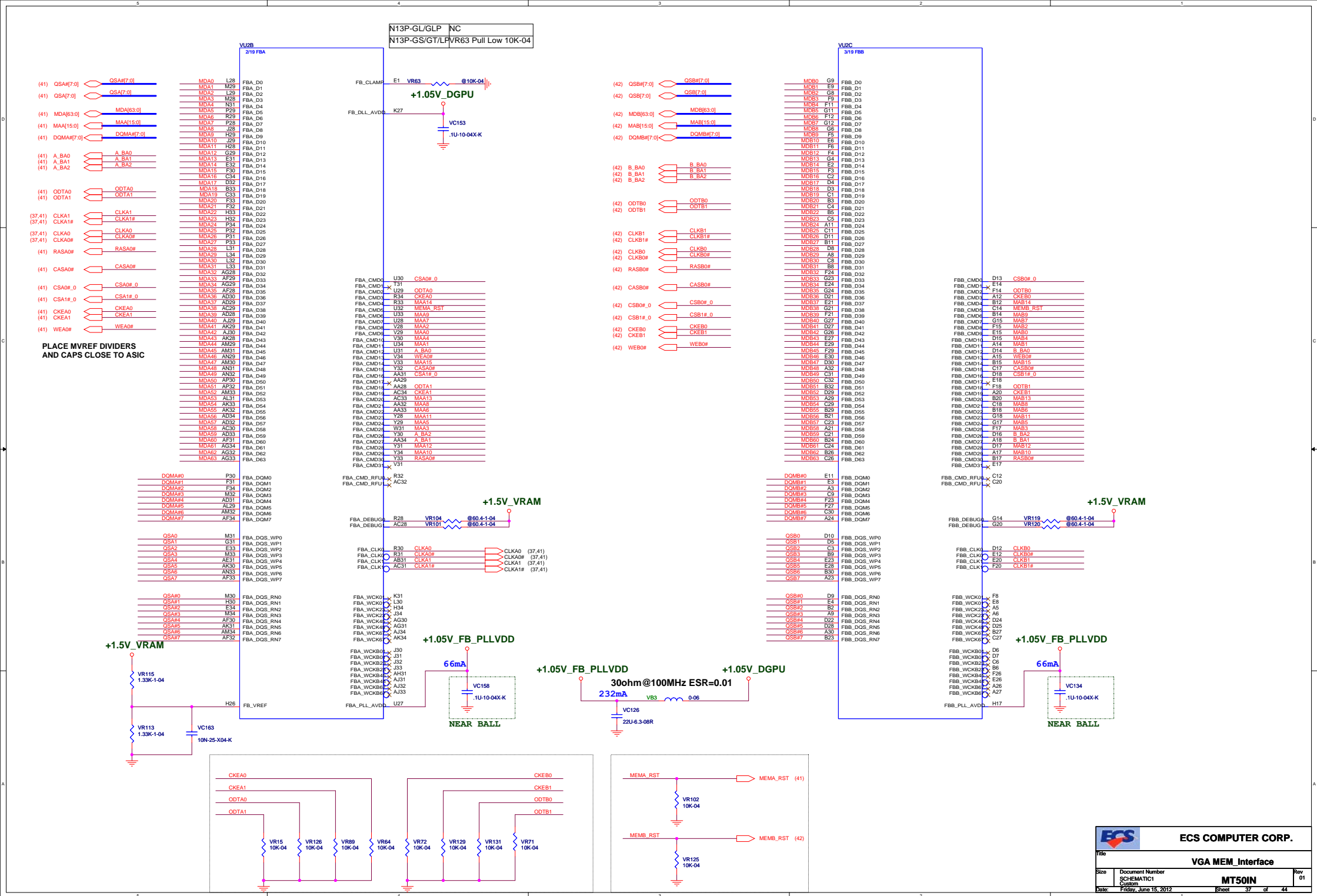
Sheet

35

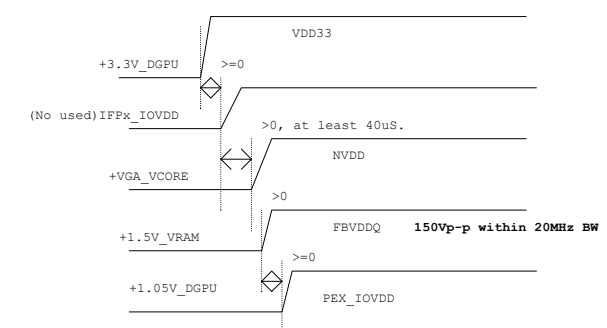
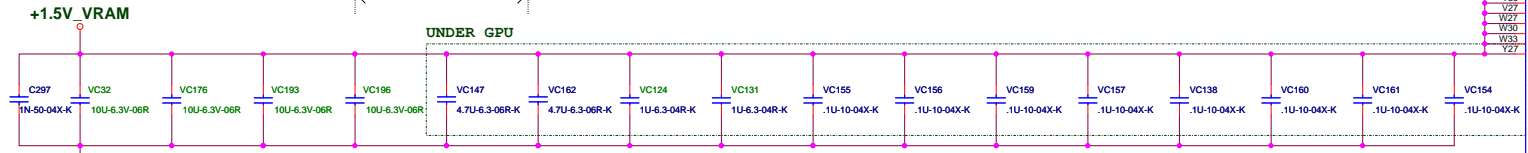
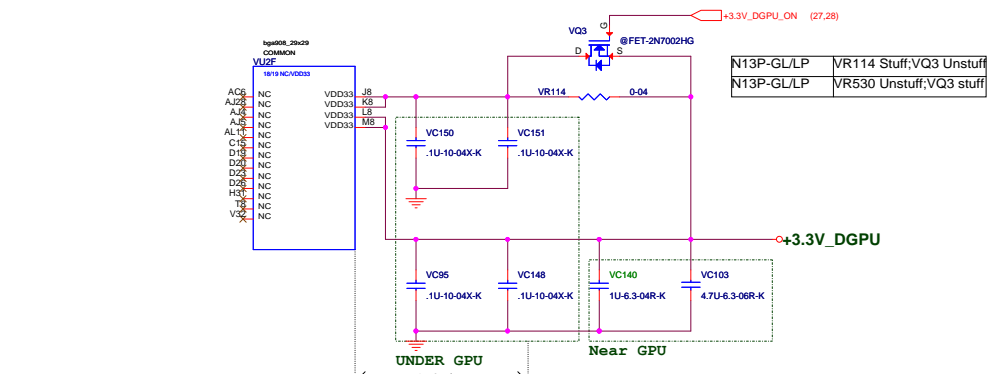
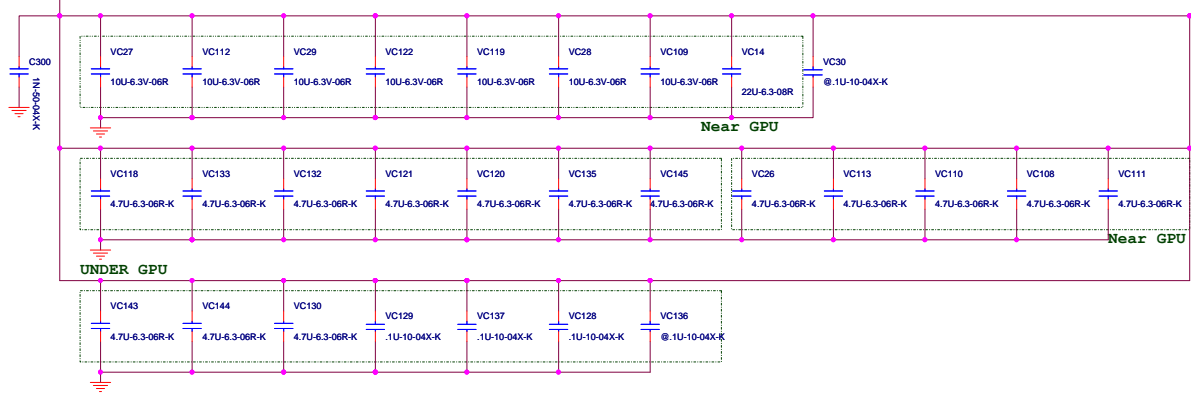
of

44

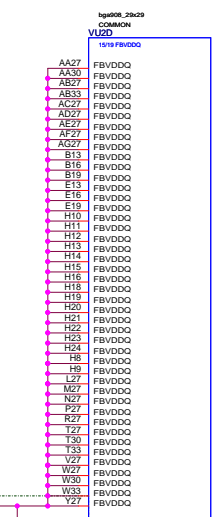
MT50IN



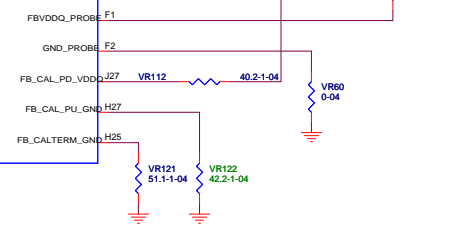
+VGA_CORE

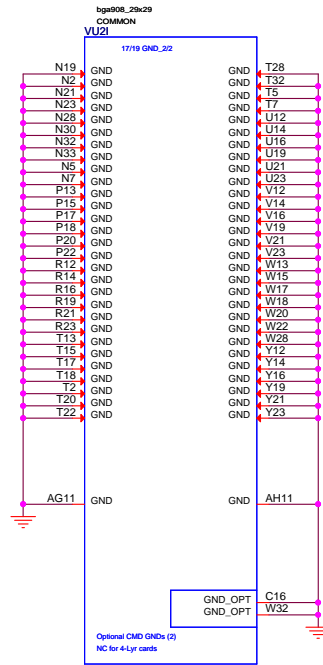
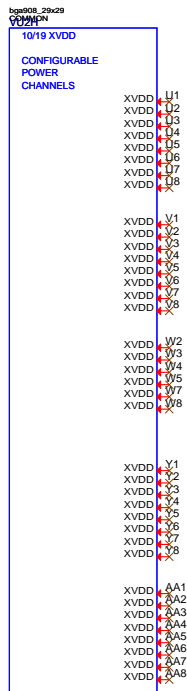
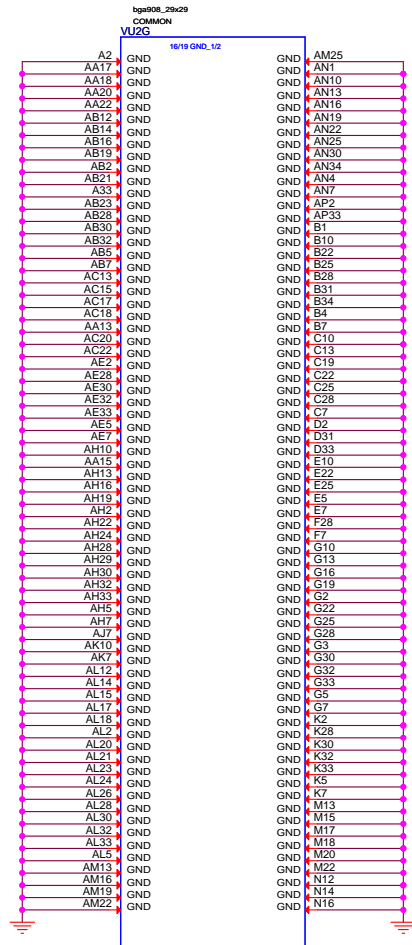


Vendor ID:10DE
Device ID:0DE9h

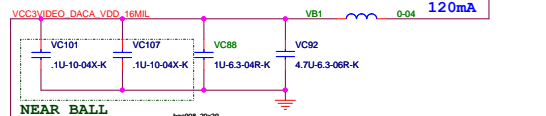


+1.5V_VRAM





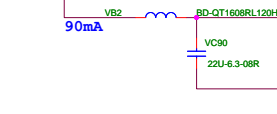
220ohm@100MHz ESR=0.05ohm
+3.3V_DGPU



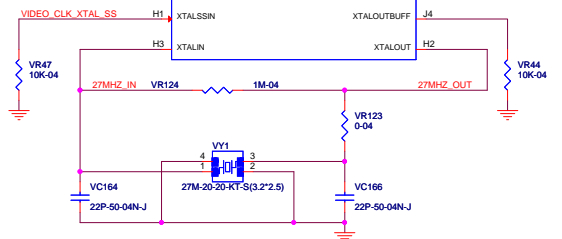
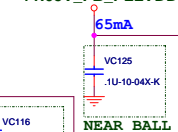
+3.3V_DGPU
Adding pull high VR141, VR142



+1.05V_DGPU
180ohm@100MHz ESR=0.2
90mA



+1.05V_FB_PLLVDD



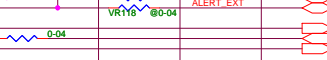
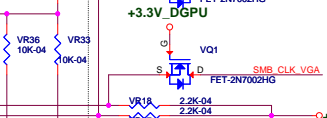
Resistance Values	PH (Pull-up to VDD3)	PL (Pull-down to GND)
5K	1000	0000
10K	1001	0001
15K	1010	0010
20K	1011	0011
25K	1100	0100
30K	1101	0101
35K	1110	0110
40K	1111	0111

I2CA=>CRT, I2CC=>LVDS.

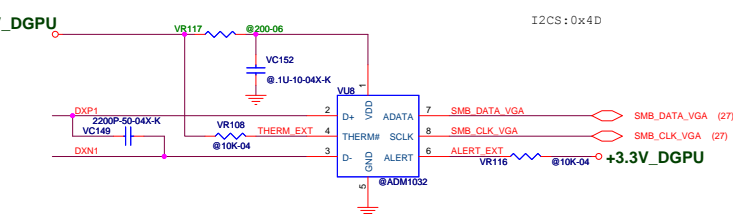
GPU Internal VGA sensor



+3.3V_DGPU
+3.3V_DGPU



External VGA Thermal Sensor



External VGA Thermal sensor	VU8, VR117, VC152, VR107, VR118 Stuff, VQ1, VQ2 Unstuff	
GPU Internal Thermal sensor	VQ1, VQ2 Stuff, VU8, VR117, VC152, VR107, VR118 Unstuff	Default

PWR_LEVEL
AC Power Detect Input :
High= AC, Low= Battery

+3.3V_DGPU

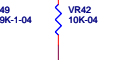
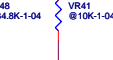
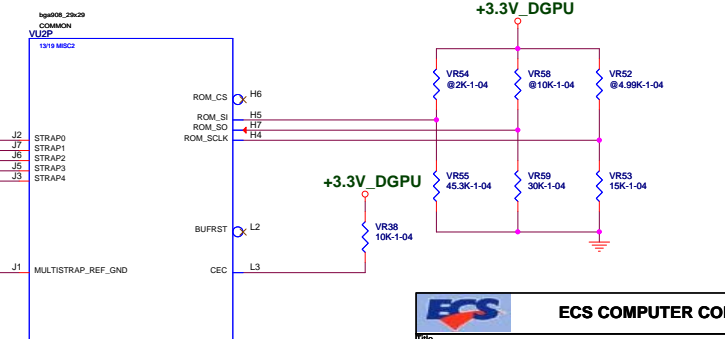


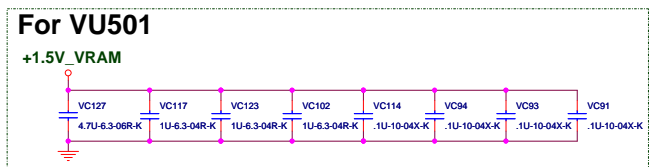
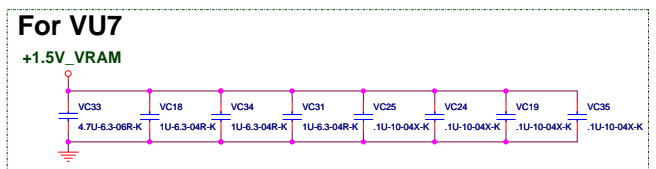
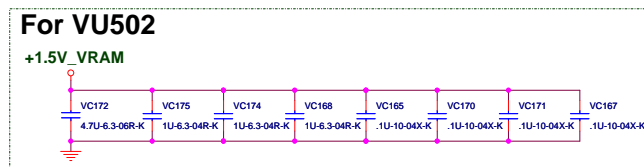
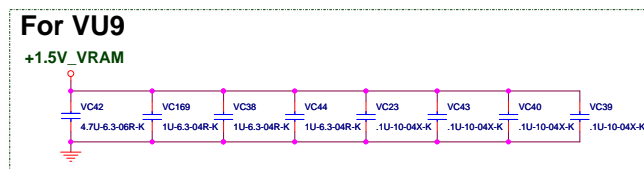
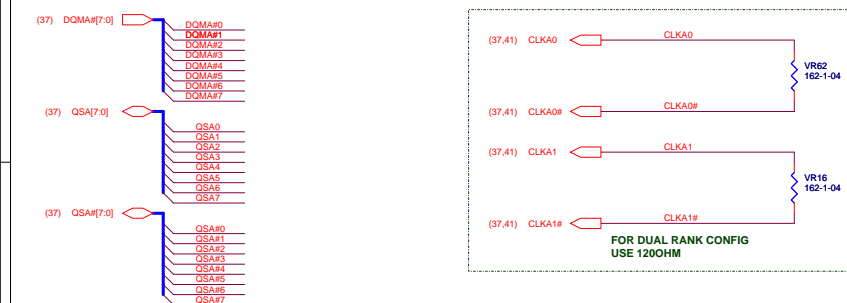
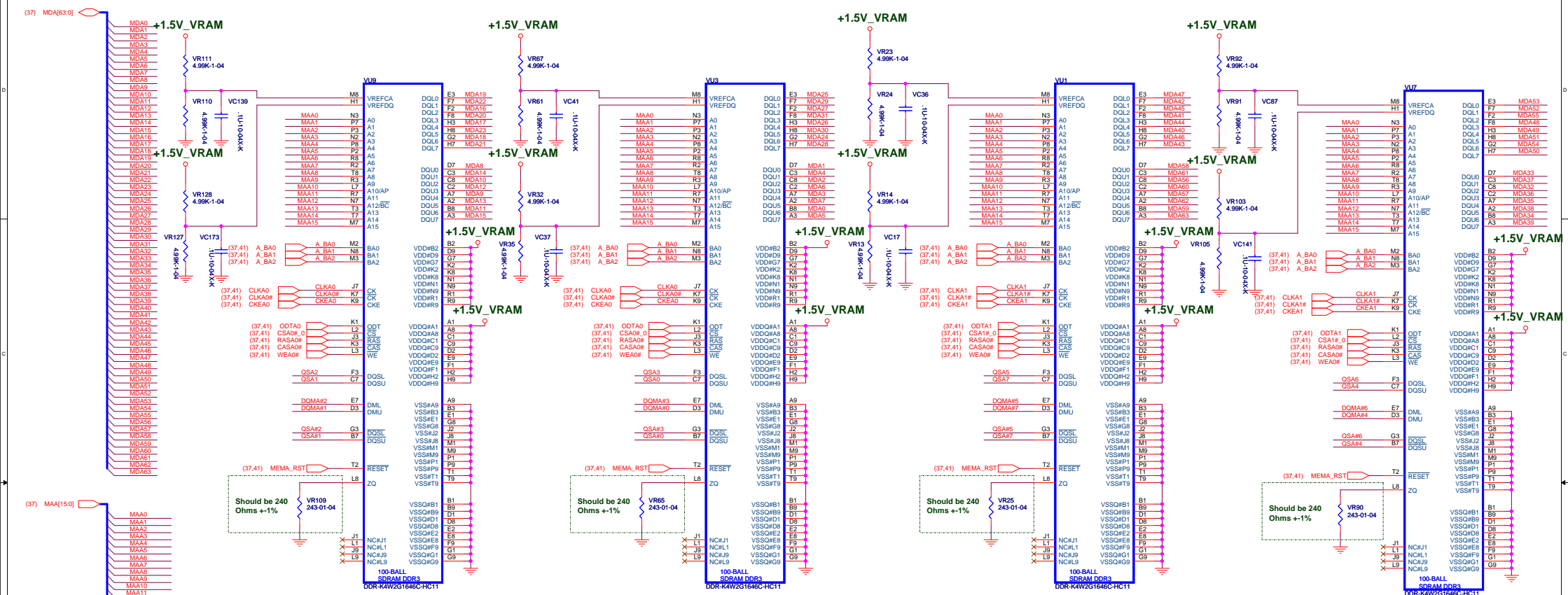
TABLE VIDEO MEMORY	HYNIX 64Mx16 0010	SAMSUNG 64Mx16 0011	HYNIX 128Mx16 0110,0101	SAMSUNG 128Mx16 0111,0100
ROM_SI VR55	15Kohm(PL)	20Kohm(PL)	34.8Kohm(PL)->B die 30Kohm(PL)->d die	C-die 45.3Kohm(PL) E-die 25Kohm(PL)
MT50IN				Default

GPU Chipset	Device ID	SCLK	Strap2	SO	NOTE
N13P-GL	0x0DE9h	PL15K	PH10K	PL30K	Default
N13P-GS	0x0FD2h	PH5K	PL15K	PH10K	
N13P-GT	0x0FDBh	PH5K	PH20K	PH10K	
N13P-GLP	0x0DE8h	PL15K	PH5K	PL30K	
N13P-LP	0x0FD3h	PH5K	PL20K	PH10K	

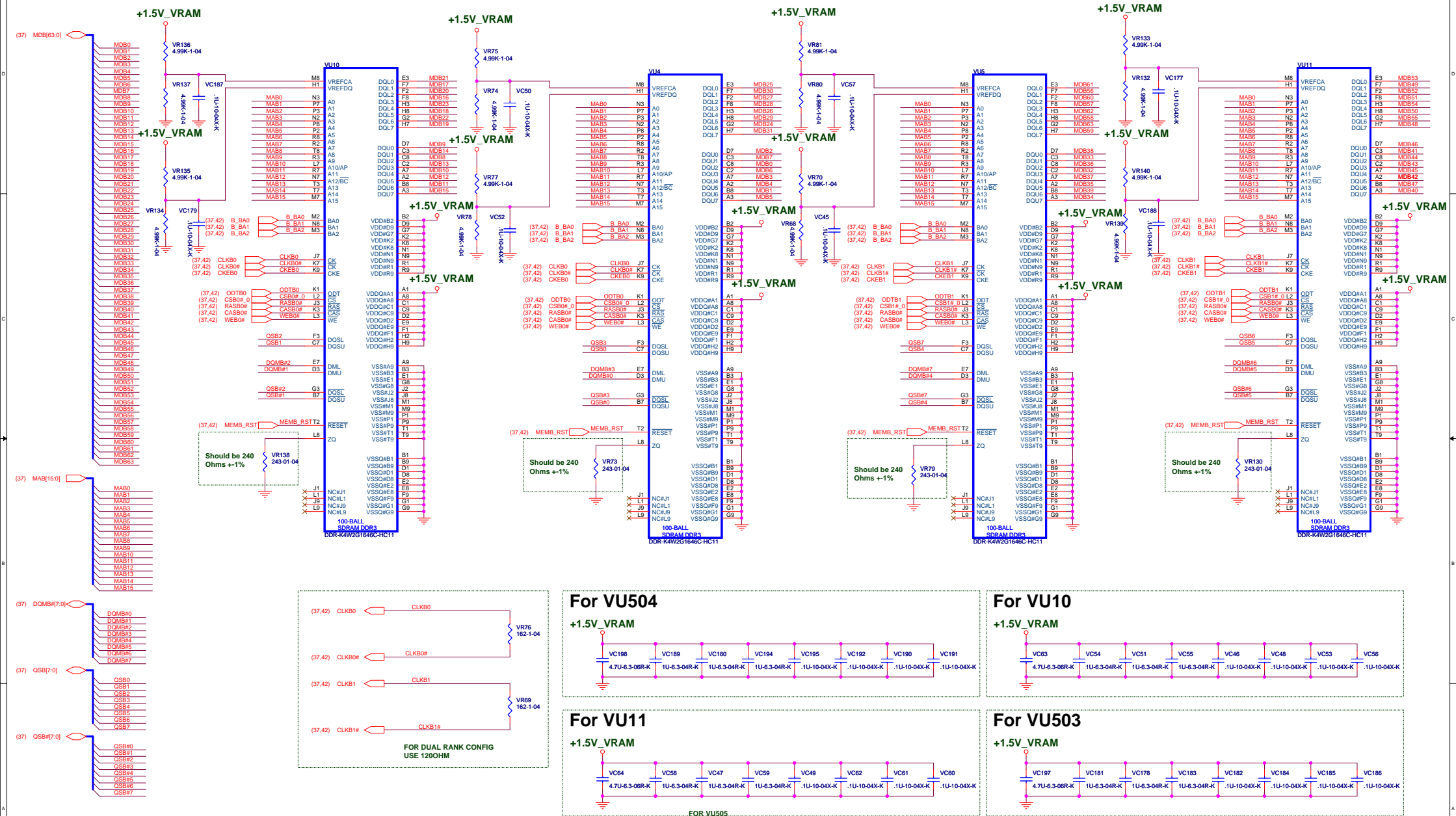
PU	PD	PIN	Multi-level Straps
45.3K		strap[0]	USER[3:0]
	45.3K	strap[1]	3GIO_PADCFG_LUT_ADR[3:0]
10K		strap[2]	PCI_DEVID[3:0]
	4.99K	strap[3]	SOR_EXPOSED[3:0]
	10K	strap[4]	RSV, PCIE_SPEED_CHANGE_GEN3, PCIE_MAX_SPEED, DP_PLL_VDD33V



CHANNEL A: 256MB/512MB DDR3 (RANK0)

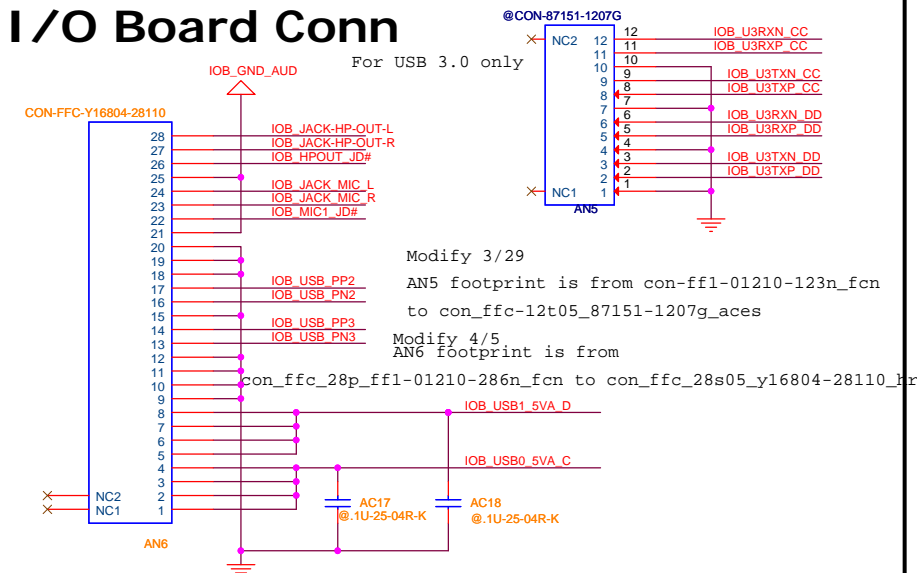


CHANNEL B: 256MB/512MB DDR3 (RANK1)

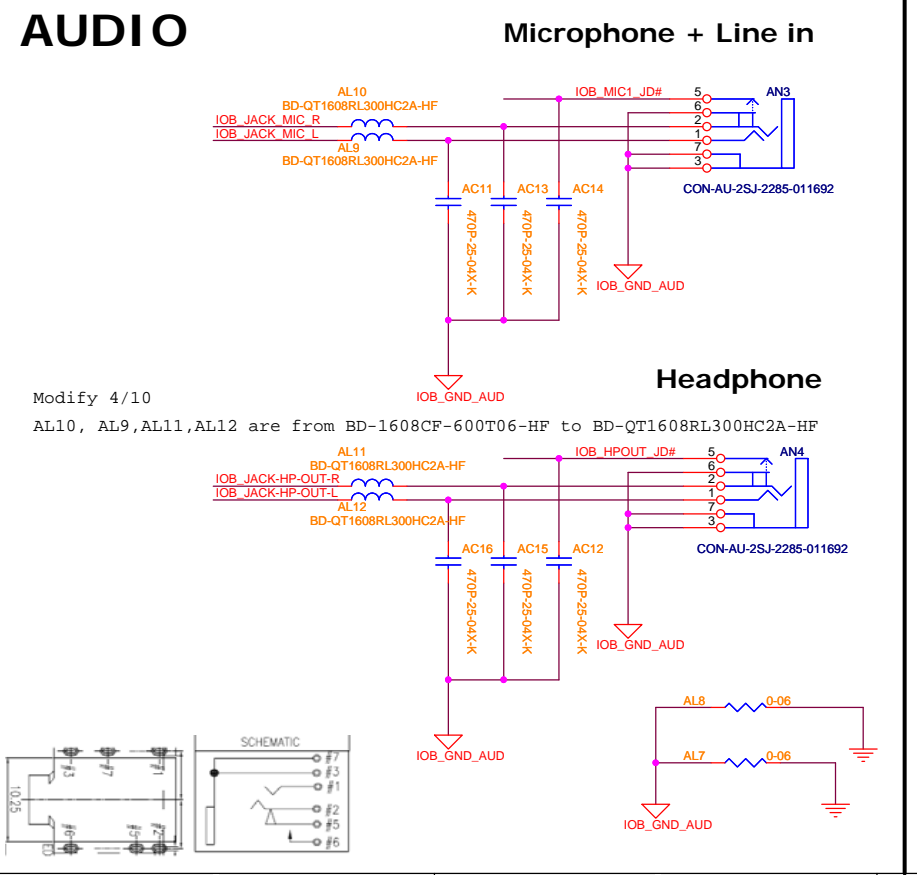


REV.	REVISION DESCRIPTION	REV.	REVISION DESCRIPTION
00	MT50IN VER:A0 Initialization		<p>PJP2,PJP17,PJP5 are from TOPCLOSE-3MM to TOPCLOSE-4MM for power request R542,R545,R543 are from 0 to BD-FBMA-11-100505-301T C452,C451,C458 are from .1uF to NC L27,L29,L30,L28 footprint is from ATCM3216 to CHOKE-4P_2X1_2X1_2 Adding PR289, connect PR8. with 8153_AGND. CN2 package change for ME request CN23 package change for ME request Delete a pin for LED6,LED7 PR227 is from 1.47K to 1.13K for OCP 50A at 80degree c, OCP 60A at 50degree c. PC81 is from NC to 6.8N for transient response PJP17 is from TOPCLOSE-4MM to TOPOPEN-4MM U4 footprint is con_cpu-pz98921-3622-01h_fox from to MPGA989_MCP_SKT_37-5MM_SQ</p> <p>Material change after gerber out to modify 4/12 Disable AOAC function, delete R541 Disable AOAC function, delete L50 mount up L49 Disable AOAC function, delete L11 mount up L12 Disable AOAC function, Stuff L49, L12, R456, R457, R458, R461, Unstuff D6, L50, L11, R467 Disable debug function, delete R456, adding R467 for BT enable function</p> <p>PR73 is from 6.04K to 499 for power request PR225 is from 2.67K to 0 for power request, disable load line function PC177 is from 2.67K to 0 for power request, disable load line function</p> <p>R21 is from 0 to BD-FBMA-11-100505-301T for EMI request</p>
01	MT50IN VER:B0 VR85 is from M-R0402 to M-R0603 PL8 is package from choke-14x12_9x5 to choke-14x12_9x3_5 for MT50IN1 PD4, MPD1 Package change from SOD123H to SOD-123H CN24 Adding U13 Package change from M-SOP8B to sop8-5_3x5_3x2_2 U16 Package change from M-S08 to sop8-5_3x5_3x2_2 Near to PJP22.2 of net +0.85V_VCNTL change to +1.5VS_VIN_PU11 Adding C454, C453, C452, C451 for reserved SATA function U5.AN24 change from +3.3V to +3.3VS R291.1 change from +1.05V to +1.8V Adding PC225, PC225 is from 33nF to NC PC139 is from NC to .1uF/25V PR71 is from 270K to 16K PR42 is from 1.91K to 2.26K for Loadline setting 1.9mQ PR51 is from 453 to 604 for GFX's power unit setting OCP 64.5A Adding PC226, PC227, PC228, PC229, PC230, PC231 Adding PC70 for power request on material Adding PC232, PC233, PC234, PC235 PR272 is from 120K to 160K for +1.5VS's power unit setting OCP 20.5A PR28 is from 0 to NC PR8 is from 26.1K to 24K for enhance +1.05V PR9 is from 137K to 124K for enhance +1.05V PR18 is from 71.5K(OCP=6A) to 12.7K(OCP=24A) PR17 is from 162K(OCP=11A) to 56K(OCP=17.6A) Removed PQ17, PR140 Modify circuit as show in figure 1 block, PQ14, PQ10 change M-SOT23G to M-SOT23A PC92 is from 1nF to 2.2nF Adding PC236, PC237 Adding pull high VR141, VR142 R336.1 of net name "SATA_LED#" change to "SATA_LED2#" Adding Q36, R540, R541 Adding R542, R544, R545 for EMI damping Adding C452, C451, C458 for EMI R128 is from 22 to 220 for EMI request C52 is from 22p to 27p for EMI request CN22 is from con_ffc_28p_ffl-01210-286n_fcn to con_ffc_28s05_y16804-28110_hr LED6, LED7 are led_2b_1tst-cl93tbkt-5a_1on from to led_2b_list-s320tbkt_1on GFXCORE6VCCCORE adding snubber solution for power request PR216, PR212, PR210 are from NC to 2.2 for snubber power request PC156, PC160, PC159 are from NC to 2200p for snubber power request +1.5VS adding snubber solution for power request PR284 is from NC to 2.2 for snubber power request PC224 is from NC to 2200p for snubber power request +1.05V4+5VA adding snubber solution for power request PR201, PR195 are from NC to 2.2 for snubber power request PC142, PC133 are NC to 2200p for snubber power request VGA Core adding snubber solution for power request PR93 is from NC to 2.2 for snubber power request PC83 is from NC to 2200p for snubber power request Modify power jumper need to close Removed PJP16,PJP15,PJP11,PJP10,PJP9,PJP23,PJP13,PJ1, PJP14,PJ2,PJP17,PJP2,PJP5,PJP3,PJP4,PJP6,PJP22,PJP19,PJP8,PJP21,PJP18 Adding PC240 for power request Adding a pin for LED6,LED7 Recovery power jumper and modify close Recovery PJP16,PJP15,PJP11,PJP10,PJP9,PJP23,PJP13,PJ1, PJP14,PJ2,PJP17,PJP2,PJP5,PJP3,PJP4,PJP6,PJP22,PJP19,PJP8,PJP21,PJP18 VR85 change material PD4, MPD1 package change from M-SOD123 to SOD-123H Cancel the connection with together, mount up L27, L29, L30, L28 for EMI request PC241, PC242 move to +1.05V Q12, Q13 are from 2N7002HG to 2N7002K for CEC issue. R199, R201 are from 100K to 10K for DDC rising time issue R470 is from 0 to 10K L27, L29, L30, L28 are from NC to CMF2012H3-900-2P-T L10,L9,L8,L7 are from CK-MCM2012B900GBE to CK-CMF2012F-900-2P-T for EMI request L27,L29,L30,L28 are from CM2012H3-900-2P-T to CMF2012H2-900-2P-T	02	MT50IN VER:01 Modify 5/21 <ol style="list-style-type: none">LED7, LED5, LED6 are footprint from led_2w_ltw-020zdcg-e2_1on to led_2b_12-21bhcc-z1lm2ry2c_ev1Adding LED8, LED9, R544, R546CN24 of connect need to swap.CN5 is from CON_ODD-S235R_1759952-3_TYC to con_odd-s235r_c18548-11305-1_at Modify 5/22 <ol style="list-style-type: none">CN5 of circuit libraery had modify gnd pin as follows layout libraryModify ID2, adding SW4, SW5 Modify 6/6 GFX side PR67 is from 680 to 576 for adjusting GFX OCP AX6618ESA material change for failrate PU11 is from AX6618ESA to APAPB8979 on material Modify 6/15 Q13, Q12 are from 2N7002K to P22N7002M R184, R195 are from 2.2K to 1K R199, R201 are from 10K to 100K

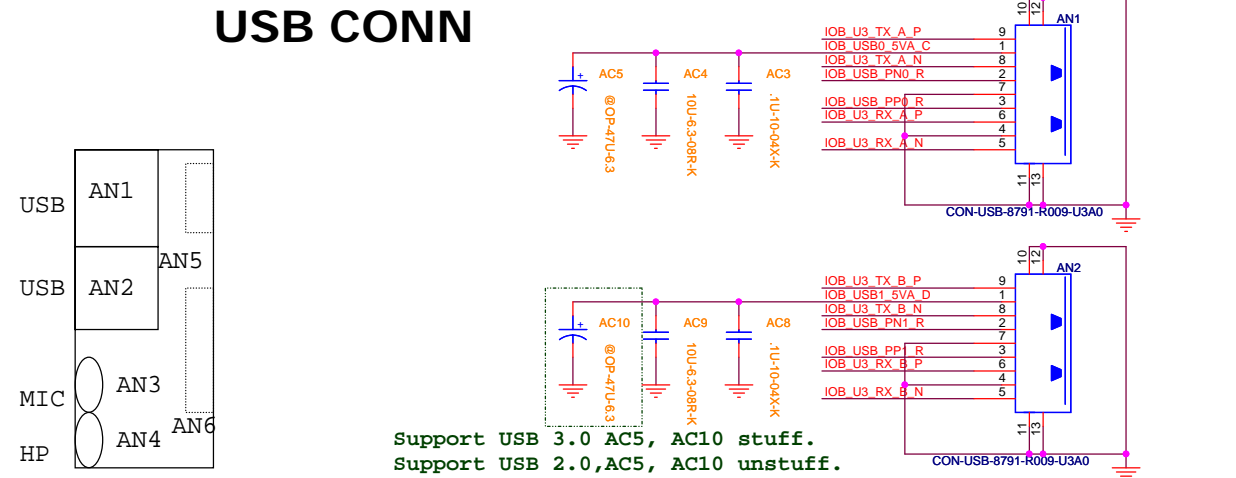
I/O Board Conn



AUDIO

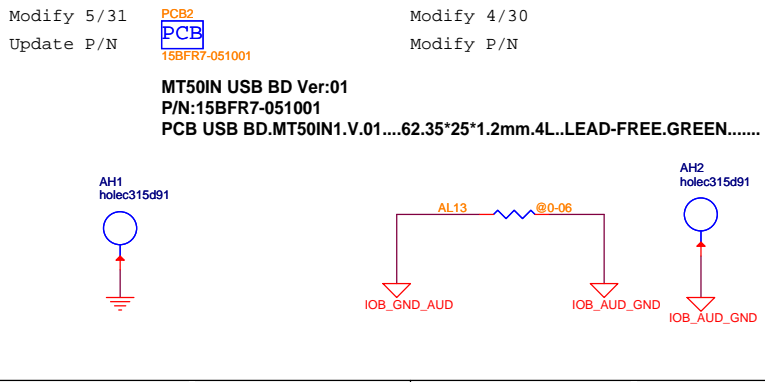
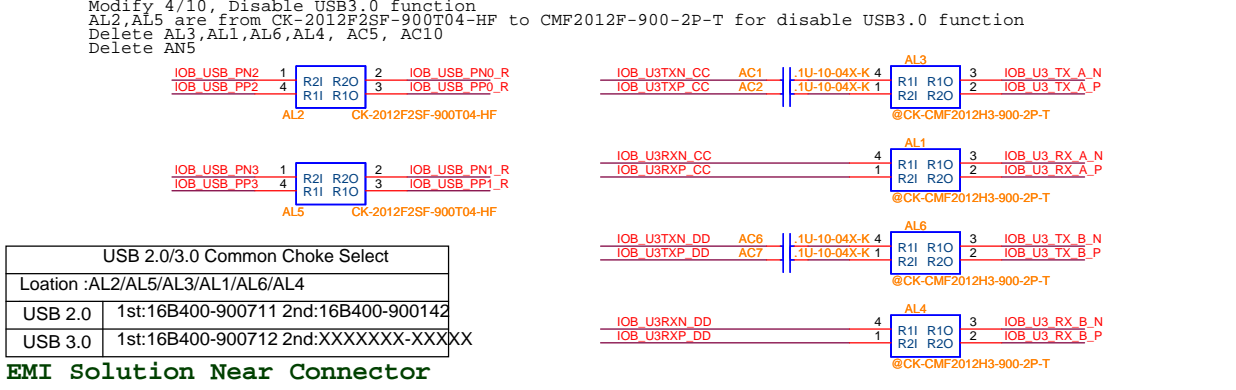


USB CONN



EMI Issue

PCH USB 2.0 Port 0 & Port 1 PCH USB 3.0 Port A & Port B



ECS COMPUTER CORP.		
Title: USB/ MIC / Headphone		
Size: Document Number	Rev 01	
Custom	MT50IN USB BD	
Date: Tuesday, July 24, 2012	Sheet	1 of 6

- 54321
- Modify 3/29
1. AN5 footprint is from con_ff1-01210-123n_fcn to con_ffc-12t05_87151-1207g_aces

2. AN6 footprint is from con_ffc_28s05-ff1-01210-fcn to con_ffc_28p_ff1-01210-286n_fcn

Modify 4/5

AN6 footprint is from con_ffc_28p_ff1-01210-286n_fcn to con_ffc_28s05_y16804-28110_hr

Modify 4/10

AL10, AL9,AL11,AL12 are from BD-1608CF-600T06-HF to BD-QT1608RL300HC2A-HF

Modify 4/10, Disable USB3.0 function

1. Delete AL3,AL1,AL6,AL4, AC5, AC10

2. AL2,AL5 are from CK-2012F2SF-900T04-HF to CMF2012F-900-2P-T for disable USB3.0 function

3. Delete AN5

Modify 4/30

Modify P/N

Modify 5/31

Update P/N

Modify 4/30
Modify P/N

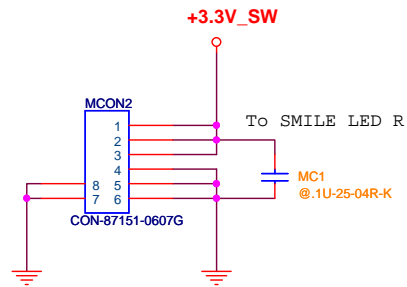
PCB3
PCB
15BFR7-051000

Modify 5/31
Update P/N

MT50IN SW BD Ver:01
P/N:15BFR7-051000
PCB SWITCH BD.MT50IN1.V.01.....30*15.3*1.2mm.4L..LEAD-FREE.GREEN.....

Modify 5/2

Removed MR2, MD1 for ME request "spacing"



Modify 4/10

MD2 footprint is from led_2b_list-s320tbkt_lon to led_2w_ltw-020zdcg-e2_lon for ME request

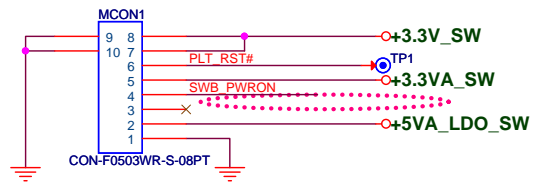
Modify 4/27

MD2 is from led_2w_ltw-020zdcg-e2_lon to led_2b_list-s320tbkt_lon for ME request

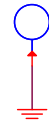
Modify 5/2

MD2 is footprint from led_2b_list-s320tbkt_lon to led_2b_12-21bhc-z11m2ry2c_ev1

SW Board Connector



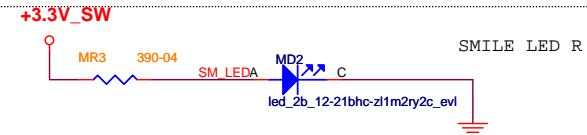
SWH1
HOLEC197D91



SWH2
HOLEC197D91-1



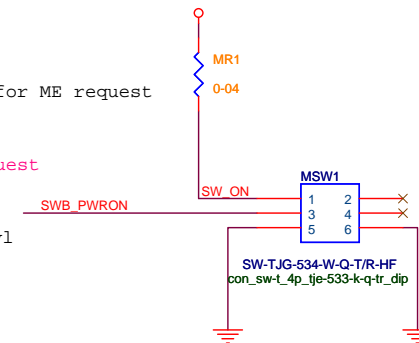
Modify 5/31
SWH1 is from holec217d91 to HOLEC197D91
SWH2 is from holec237d91 to HOLEC197D91-1



Modify 4/9

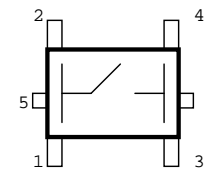
MD2 is from led_2b_1tst-c193tbkt-5a_lon to led_2b_list-s320tbkt_lon, and adding a pin

+5VA_LDO_SW




Modify 4/11

MSW1 material change for ME request



Top View

		ECS COMPUTER CORP.	
Title		Power SW/LED	
Size	Document Number	MT50IN SW BD	Rev 01
Date:	Tuesday, July 24, 2012	Sheet 3 of 6	

Modify 4/10
MD2 footprint is from led_2b_list-s320tbkt_lon to led_2w_ltw-020zdcg-e2_lon for ME request
Modify 4/11
MSW1 footprint is from con_sw-t_4p_tje-533-k-q-tr_dip to con_sw-t_tje-533i-q-tr12_dip for ME request
MSW1 material change for ME request
Modify 4/27
MD2 is from led_2w_ltw-020zdcg-e2_lon to led_2b_list-s320tbkt_lon for ME request
Modify 4/30
Modify P/N
Modify 5/2
Removed MR2, MD1 for ME request "spacing"
Modify 5/2
MD2 is footprint from led_2b_list-s320tbkt_lon to led_2b_12-21bhc-zllm2ry2c_evl
Modify 5/31
Update P/N
SWH1 is from holec217d91 to HOLEC197D91
SWH2 is from holec237d91 to HOLEC197D91-1

LED BD Left Side

Modify 4/30

Modify P/N

PCB4
PCB
15BFR7-051002

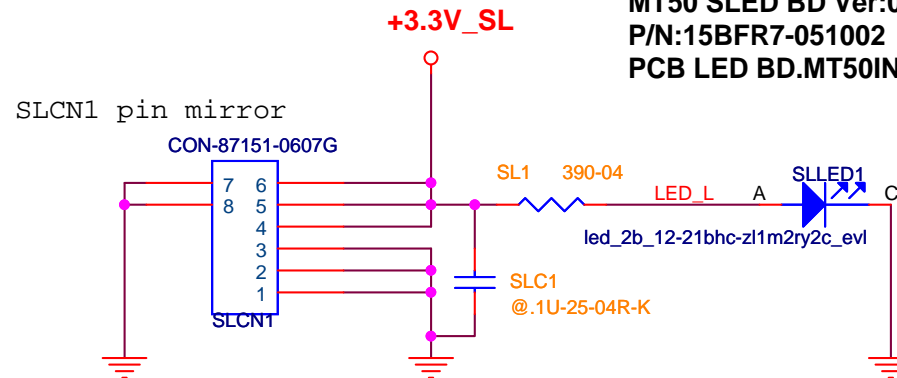
Modify 5/31

Update P/N

MT50 SLED BD Ver:01

P/N:15BFR7-051002

PCB LED BD.MT50IN1.V.01....36*13*1.2mm.4L..LEAD-FREE.GREEN.....



Modify 4/5

SLED1 is from led_2b_ltst-c193tbkt-5a_lon to led_2b_list-s320tbkt_lon

Modify 4/6

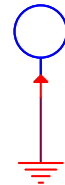
Adding a pin for SLLED1

Modify 5/2

SLLED1 is footprint from led_2b_list-s320tbkt_lon to led_2b_12-21bhc-z1m2ry2c_ev1

SLH1
HOLEC237D91

SLH2
HOLEC237D91



Modify 4/10

SLLED1 footprint is from led_2b_list-s320tbkt_lon to led_2w_ltw-020zdcg-e2_lon for ME request

Modify 4/27

SLLED1 is from LED_2W_LTW-020ZDCG-E2_LON to led_2b_list-s320tbkt_lon for ME request



ECS COMPUTER CORP.

Title

LED

Size

Document Number

SCHEMATIC1

MT50IN LED BD

Rev

01

Date:

Tuesday, July 24, 2012

Sheet

5

of

6

EE Schematics Modify

Modify B phase

SLED1 is from led_2b_ltst-c193tbkt-5a_lon to led_2b_list-s320tbkt_lon for ME request

Adding a pin for SLLED1

SLLED1 footprint is from led_2b_list-s320tbkt_lon to led_2w_ltw-020zdcg-e2_lon for ME request

Modify 4/27

SLLED1 is from LED_2W_LTW-020ZDCG-E2_LON to led_2b_list-s320tbkt_lon for ME request

Modify 4/30


Modify P/N

Modify 5/2

SLLED1 is footprint from led_2b_list-s320tbkt_lon to led_2b_12-21bhc-z11m2ry2c_ev1

Modify 5/31

Update P/N

		ECS COMPUTER CORP.	
Title			
Change Notes			
Size	Document Number	Rev	
	SCHEMATIC1	01	
	A	MT50IN LED BD	
Date:	Tuesday, July 24, 2012	Sheet	6 of 6